

## **PRITH BANERJEE**

Dean, College of Engineering and  
UIC Distinguished Professor  
University of Illinois at Chicago

### **ADDRESS:**

#### **Office:**

University of Illinois at Chicago  
Room 838 SEO  
851 South Morgan Street  
Chicago, IL 60607-7043  
Ph: (312) 996-8249  
Fax: (312) 996-8664  
Cell: (847) 757-8708  
EMAIL: [prith@uic.edu](mailto:prith@uic.edu)  
URL: [www.uic.edu/~prith](http://www.uic.edu/~prith)

#### **Residence:**

2130 Chandler Lane  
Glenview, IL-60026  
(847) 657-8749

**PERSONAL:** Born July 17, 1960, U.S. citizen, married, one son.

### **EDUCATION:**

- Ph.D. (Dec. 1984), Electrical Engineering, University of Illinois, Urbana
- M.S. (Dec. 1982), Electrical Engineering, University of Illinois, Urbana
- B.Tech. (Jun. 1981), Electronics and Electrical Eng., Indian Institute of Technology, Kharagpur

### **WORK EXPERIENCE:**

- Aug. 2004-present, University of Illinois at Chicago, Dean, College of Engineering, and UIC Distinguished Professor of Electrical and Computer Engineering and Computer Science. Responsible for six academic departments, 115 faculty, 1550 undergraduate students, and 900 graduate students.
- July 2004-present, BINACHIP, Founder , Chairman and Chief Scientist. Responsible for providing technical leadership for the company.
- 1998 - 2001, and 2002-2004, Northwestern University, Chairman and Walter Murphy Professor, Electrical and Computer Engineering. Responsible for a department with 31 faculty, 120 graduate students, 250 undergraduate students; Instrumental in developing some novel undergraduate curriculum revisions, strong industrial interactions, and collaborative research funding.
- 1996 - 2004, Northwestern University, Director, Center for Parallel and Distributed Computing. Responsible for building a center with 12 faculty, being a principal investigator of five large research projects with more than \$8 million in funding from DARPA, NSF, NASA, DOE, and others.
- July 2002 – June 2004, AccelChip, Inc, Founder and Chief Scientist. Responsible for providing technical leadership for the company. AccelChip was purchased by Xilinx in Jan. 2006.
- July 2000 - June 2002, AccelChip, Inc., Founder, President and CEO. Responsible for founding the company, raising \$2.3 million in Venture Capital funding, hiring a top management team, growing the company to about

25 employees, developing the first product AccelFPGA, and generating more than \$800,000 in revenue. AccelChip was purchased by Xilinx in Jan. 2006.

- 1994-1996, University of Illinois, Director, Computational Science and Engineering. Responsible for building a CSE graduate program in 10 engineering departments setting up a CSE lab, and coordinating the writing of several large research proposals.
- 1993-1996, University of Illinois, Professor, Electrical and Computer Eng, Professor, Coordinated Science Laboratory. Supervised more than 25 Ph.D. and 20 M.S. students, and had four large research projects.
- 1989-1993, University of Illinois, Associate Professor, Electrical and Computer Engg. Research Associate Professor, Coordinated Science Laboratory.
- 1985-1989, University of Illinois, Assistant Professor.

#### **AWARDS AND HONORS:**

- Elected Fellow of the American Association of Advancement of Science (AAAS), 2006.
- UIC Distinguished Professor, from University of Illinois at Chicago, 2004
- Received the Taylor Booth Award for Outstanding Educator in the field of Computer Science and Engineering, awarded by the IEEE Computer Society, 2001.
- Elected Fellow of Association of Computing Machinery (ACM), 2000
- Awarded the Best Paper Award at the Int. Symp. on Parallel and Dist. Systems, Cancun, MX, May 2000.
- Awarded the Best Paper Award at the IEEE VLSI Test Symposium, Monterey, CA, April 1998.
- Recipient of the 1996 Frederick Emmons Terman Award from the ASEE's Electrical Engineering Division, sponsored by Hewlett-Packard Company, presented to an Outstanding Young Electrical Engineering Educator, for publishing the textbook "Parallel Algorithms for VLSI CAD".
- Walter Murphy Chaired Professor, Northwestern University, 1996
- Elected Fellow of Institution of Electronics and Electrical Engineers (IEEE), 1995
- Awarded the 1994 Outstanding Paper Award from the International Conference on Parallel Processing, St. Charles, IL, August 1994.
- Awarded the 1992 University Scholar Award from the University of Illinois.
- Recipient of the 1992 Senior Xerox Award for Faculty Research, University of Illinois.
- Awarded the National Science Foundation's Presidential Young Investigator Award 1987.
- Awarded the IBM Young Faculty Development award for research in Computer Engineering, 1986.
- Recipient of the IBM Graduate Fellowship in Computer Science, 1983 and 1984.
- Awarded the President of India Gold Medal for highest rank among all disciplines the Indian Institute of Technology, Kharagpur, 1981.

## REPORTED IN THE NEWS:

- Chicago Tribune, March 20, 2006  
<http://www.chicagotribune.com/entertainment/shopping/chi-0603200154mar20,1,5189972.story?track=rss&ctrack=1&cset=true>
- EE Times, March 20, 2006  
<http://www.eetimes.com/news/design/showArticle.jhtml;jsessionid=421LBSNNHMZBEQSNDBCSKHSCJU MEKJVN?articleID=183700831>
- Chicago Tribune, Jan. 4, 2006  
<http://www.chicagotribune.com/news/local/chi-060103uicgift,1,6125818.story?ctrack=1&cset=true>
- Chicago Sun Times, Jan. 4, 2006  
<http://www.suntimes.com/output/news/uic03.html>
- Crain's Chicago Business, Jan. 3, 2006  
<http://www.chicagobusiness.com/cgi-bin/news.pl?id=18985>
- Crain's Chicago Business, Feb. 7, 2005  
<http://www.chicagobusiness.com/cgi-bin/register.pl?bridge=1>
- Chicago Sun Times, June 4, 2004  
<http://www.suntimes.com/output/news/cst-nws-dean04.html>
- Hindustan Times, June 5, 2004  
[http://www.hindustantimes.com/news/5967\\_805523.00160006.htm](http://www.hindustantimes.com/news/5967_805523.00160006.htm)
- Electrical Engineering Times (EE Times), May 2003  
<http://www.eedesign.com/news/OEG20030507S0036>
- Electronic Design, June 2002  
<http://www.e-insite.net/electronicnews/index.asp?layout=article&articleId=CA223041%20>
- Electronic News, Apr. 2002  
<http://www.e-insite.net/electronicnews/index.asp?layout=article&articleId=CA209256>
- Electrical Engineering Times (EE Times), Apr. 2002  
<http://www.eedesign.com/story/OEG20020402S0049>
- Electrical Engineering Times (EE Times), Article on MATCH Compiler, Aug. 2000  
<http://www.eet.com/story/OEG20000810S0021>
- Electrical Engineering Times (EE Times), Article on PACT Compiler, Aug. 2000  
<http://www.eet.com/story/OEG20000817S0008>

## RESEARCH CONTRACTS AND GRANTS:

- National Science Foundation, (Co-Principal Investigator with David Zaretsky), "Automated Design Environment for Embedded Systems," \$100,000, 2006-07.
- Intel Corporation, (Principal Investigator), "A Hardware/Software Codesign Environment for Low Power Embedded Systems," (Principal Investigator), \$100,000, 2006-08.
- JSC Global, (Principal Investigator), "Software Technology Center," \$60,000, 2006-07.

- Department of Energy, (Principal Investigator), "An Integrative Bio-engineering Institute." \$722,000, 2006-07.
- National Aeronautics and Space Administration (NASA) (Co-Principal Investigator with David Zaretsky), "A Hardware/Software Design Environment for Reconfigurable Communications Systems," \$69,300, 2006.
- National Aeronautics and Space Administration (NASA) (Principal Investigator), "A System Level Tool for Translating Software to Reconfigurable Hardware," \$100,000, 2005-06.
- Calypto Design Systems, (Principal Investigator), "System Level Verification Algorithms," \$33,000, 2004-05.
- National Aeronautics and Space Administration (NASA) (Principal Investigator), "MATLAB Based Adaptive Computing for NASA Image Processing Applications," \$309,835, 2000-04.
- Defense Advanced Research Projects Administration (DARPA) (Principal Investigator), "PACT: Power Aware Architectural and Compilation Techniques," \$1,202,906, 2000-2003.
- Synplicity Corporation (Principal Investigator), "Software Tools for FPGA and ASIC Synthesis and Verification," 2003, software donation.
- Synopsys Corporation (Principal Investigator), "Software Tools for Logic Synthesis," 2000-2002, software donation, (obtained through University Program)
- Cadence Design Systems (Principal Investigator), "Tools for Electronic Design Automation," 2000-2002, software donation, (obtained through University Program)
- Microsoft Corporation (Principal Investigator). "New Initiatives in the Electrical and Computer Engineering Department," 2000-2001, hardware, software and cash donation, \$690,000.
- Motorola Foundation (Principal Investigator), "New Initiatives in the Electrical and Computer Engineering Department," 1999-2004, cash donation, \$500,000.
- Defense Advanced Research Projects Administration (DARPA) (Principal Investigator), "A MATLAB Compilation Environment for Adaptive Computing Systems," \$1,855,662, 1998-2001.
- Department of Energy, ASCI Level-2 (Co-Principal Investigator), "Large High-Performance Data Management, Access, and Storage Techniques for Tera-Scale Scientific Applications," \$876,000, 1998-2001.
- Defense Advanced Research Projects Administration (DARPA) (Co-Principal Investigator) "Architectures, Compilers, and Configuration Management of Reconfigurable Computing for Mass-Market Computing," \$1,981,349, 1997-2000.
- National Science Foundation (Principal Investigator), "A High-Speed Distributed Computing Infrastructure", \$906,512, 1997-2002.
- National Science Foundation (Principal Investigator), "Efficient Compilation Issues in Distributed Memory Multicomputers," \$94,000, 1996-99.
- Mentor Graphics Corporation (Principal Investigator), "VLSI Computer Aided Design Tools", 1996-02, software donation.
- IBM Corporation (Principal Investigator), "IBM Research Partnership Award: Parallelizing Compiler for Distributed Memory Multicomputers", \$40,000, 1995-96.
- Defense Advanced Research Projects Administration, administered by the Army Research Office, (Principal Investigator), "VLSI CAD on Scalable High Performance Computing Platforms," \$1,690,000, 1994-98.
- National Science Foundation (Principal Investigator), "Parallel Algorithms for Synthesis and Test," \$126,000, 1994-98.
- Office of Naval Research (Principal Investigator) "A Novel Approach to Fault Tolerance in Distributed Memory Multiprocessors," \$431,000, 1990-93.
- National Science Foundation (Presidential Young Investigator), "Design Issues in Parallel Processor Architectures," \$312,000, 1987-92.
- Semiconductor Research Corporation (Principal Investigator), "Reliable VLSI Architectures," \$187,500, 1987-92.
- National Science Foundation, (Principal Investigator), "Fault Tolerant Highly Parallel Signal Processing Architectures," \$46,000, 1988-89.
- National Science Foundation, (Principal Investigator), "Parallel Algorithms for VLSI Circuit Extraction on Multiprocessors," \$48,000, 1988-89.
- Office of Naval Research (Principal Investigator), "An Algorithmic Approach to Fault Tolerance in Parallel Processors for Space Applications," \$60,800, 1988-89.
- General Electric Corporate Research and Development (Principal Investigator), "Parallel Architecture and Algorithms," \$37,500, 1987-92.

- National Science Foundation Engineering Research Equipment Grant (Co-principal Investigator with Prof. Wah and Prof. Iyer), "Algorithm Development and Performance Evaluation of Hypercube Multiprocessors, \$130,000, 1987-89.
- Intel Scientific Computers (Principal Investigator), "Evaluating Parallel Algorithms on the Intel Hypercube," \$50,000, 1987-89.
- IBM Corporation (Principal Investigator), "Parallel Algorithms for VLSI Design Automation," \$60,000, 1986-88.

#### **PROFESSIONAL SOCIETIES AND ACTIVITIES:**

- Board of Directors, BINACHIP, 2004-present
- National Science Foundation CAREER Panel, 2005
- Board of Directors, AccelChip, 2000-2003
- Technical Advisory Board, Ambit Design Systems, Santa Clara, CA, 1997-1998.
- Technical Advisory Board, Atrenta, San Jose, CA, 2002-present.
- Technical Advisory Board, Calypto Design Systems, Santa Clara, CA, 2003-2005
- Associate Editor, IEEE Transactions on Parallel and Distributed Systems, 2000-2002.
- Associate Editor, IEEE Transactions on Computers, 1996-2001.
- Associate Editor, Journal of Parallel and Distributed Computing, 1993-2000.
- Associate Editor, IEEE Transactions on VLSI Systems, 1992-1996.
- Associate Editor, Journal of Circuits, Systems and Computers, 1991-1993.
- Editor, Electronic Newsletter on Fault-Tolerant Computing, 1990-92.
- Program Chairman, Int. Conf. High-Performance Computing (HIPC-99), Dec. 1999, Calcutta, INDIA.
- General Chairman, 10th Int. Conf. Parallel and Distributed Computing Systems, New Orleans, Oct. 1997.
- General Chairman, IEEE Int. Workshop on Hardware Fault Tolerance in Multiprocessors, Urbana, 1989.
- Program Chairman, 6th International Conference on High-Performance Computing, Dec. 1999, Calcutta, INDIA.
- Program Chairman, Int. Conf. Parallel Processing (ICPP-95), Oconomowoc, WI, Aug. 1995.
- Program Area Chairman, Int. Symp. Circuits and Systems (ISCAS-93), (Chicago, Illinois, May 1993).
- Advisory Committee, IASTED Conf. Parallel and Distributed Computing Systems (PDCS), Nov. 2002, MIT, Boston, MA
- Advisory Committee, IASTED Conf. Parallel and Distributed Computing Systems (PDCS), Nov. 2001, MIT, Boston, MA
- Program Committee Member, Int. Conference on High Performance Computing, Dec. 2003, Hyderabad, INDIA
- Program Committee Member, International Symp. On Parallel and Dist. Systems (ISPDS), Apr. 2002, Nice, France.
- Program Committee Member, International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES), Nov. 2001, Atlanta, GA
- Program Committee Member, Int. Conf. Parallel Processing (ICPP-00), Minneapolis, MN, Aug. 2000.
- Steering Committee Member, 11th International Conference on Parallel and Distributed Computing and Systems (PDCS'99), Boston, MA, Oct. 1999.
- Program Committee Member, Supercomputing Conference (SC-98), Nov. 1998.
- Program Committee Member, 9th Int. Conf. Architectural Support of Programming Languages and Operating Systems, (ASPLOS-98), Santa Clara, CA, Oct. 1998).
- Program Committee Member, Int. Conf. Parallel Processing (ICPP-98), Minneapolis, MN, Aug. 1998.
- Program Committee Member, Int Symp. on Computer Architecture (ISCA-98), Barcelona, Spain, Jun. 1998.
- Program Committee Member, 12th Int. Parallel Processing Symp. (IPPS-98), (Orlando, FL, Apr. 1998)
- Program Committee Member, Workshop on Communication, Architecture, and Applications for Network based Parallel Computing (CANPC 98), (Las Vegas, NE, Feb. 1998).
- Program Committee Member, 10th Int. Conf. on VLSI Design (VLSI-98), (Chennai, INDIA, Jan. 1998).
- Program Committee Member, Int. Conf. Parallel Processing (ICPP-97), (Chicago, IL, Aug. 1997).
- Program Committee Member, 11th Int. Parallel Processing Symp. (IPPS-97), (Geneva, SWITZERLAND, Apr. 1997.)

- Program Committee Member, 9th Int. Conf. on VLSI Design (VLSI-97), (Hyderabad, INDIA, Jan. 1997).
- Program Committee Member, 3rd Int. Conf. High-Performance Computing (ICHPC-96, (Trivandrum, INDIA, Dec. 1996.)
- Program Committee Member, 8th Int. Symp. on Parallel and Distributed Processing (SPDP-96) (New Orleans, LO, Oct. 1996).
- Program Committee Member, 1996 Int. Conf. Parallel Processing (ICPP-96), (Bloomingdale, IL, Aug. 1996).
- Program Committee Member, 3rd Int. Workshop on Parallel Algorithms for Irregularly Structured Problems, (Santa Barbara, CA, Aug. 1996).
- Program Committee Member, 26th Int. Symp. on Fault-Tolerant Computing (FTCS-96), (Sendai, JAPAN, June 1996).
- Program Committee Member, 10th Int. Parallel Processing Symp. (IPPS-96), Honolulu, HA, Apr. 1996. ffl Program and Organizing Committee Member, 8th Int. Conf. on VLSI Design (Bangalore, INDIA, Jan. 1996).
- Program Committee Member, Int. Conf. High Performance Computing, New Delhi, INDIA, Dec. 1995. ffl Program Committee Member, 7th Int. Symp. on Parallel and Distributed Processing (San Antonio, TX, Oct. 1995).
- Program Committee Member, 9th Int. Parallel Processing Symp. (IPPS-95), Santa Barbara, CA, Apr. 1995.
- Program Committee Member, 7th Int. Conf. on VLSI Design (New Delhi, INDIA, Jan. 1995).
- Organizing and Program Committee Member, 21st Int. Symp. on Computer Architecture, (Chicago, IL, May 1994).
- Program Committee Member, 8th Int. Parallel Processing Symp. (IPPS-94), Cancun, Mexico, Apr. 1994.
- Organizing and Program Committee Member, 6th Int. Conf. on VLSI Design (Calcutta, INDIA, Jan. 1994).
- Program Committee Member, 23rd Int. Symp. Fault Tolerant Computing (Toulouse, FRANCE, June 1993).
- Program Committee Member, 5rd Int. Conf. on VLSI Design (Bombay, INDIA, Jan. 1993).
- Program Committee Member, 19th Int. Symp. on Computer Architecture, (Queensland, Australia, May 1992).
- Program Committee Member, Int. Workshop on Fault Tolerance in Parallel and Distributed Systems, (Amherst, MA, Jul. 1992).
- Program Committee Member, 18th Int. Symp. on Computer Architecture (Toronto, CANADA, May 1991).
- Program Committee Member, 5th Int. Parallel Processing Symp. (Orange County, California, Mar. 1991).
- Program Committee Member, 3rd Int. Symp. on VLSI Design (New Delhi, INDIA, Jan. 1991).
- Organizing Committee Member, 19th Int. Symp. Fault-Tolerant Computing (Chicago, June 1989).
- Program Committee Member, 18th Int. Symp. Fault Tolerant Computing (Tokyo, June 1988).
- Presented Tutorial on "Parallel Nonnumerical Algorithms with Applications to VLSI CAD" Int. Parallel Processing Symp., Cancun, Mexico, Apr. 1994.
- Presented Tutorial on "Massively Parallel Processing", AT&T (Chicago, June 1993)
- Presented NTU Television Short Course on "Fault Tolerant Multiprocessors", (NTU, May 1994)
- Presented NTU Television Short Course on "Massively Parallel Computing", (NTU, Apr. 1993)
- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Int. Parallel Processing Symp, (Cancun, Mexico, Apr. 1993).
- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Int. Conf. Supercomputing, (Washington, DC, Jul. 1992).
- Presented Tutorial on "Introduction to Massively Parallel Processing", Univ. of Illinois Continuing Education, (Chicago, June 1992)
- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Design Automation Conf. (Orlando, FL, June 1990),
- Presented Tutorial on "Parallel Processing in VLSI Computer-Aided Design Applications," Int. Conf. Computer-Aided Design (Santa Clara, CA, 1988).
- Invited Panelist on "Launching New Products," ITEC Center, Oct. 2002.
- Invited Panelist on "Program Portability for Parallel Architectures", at IPPS-94 Conference, Cancun, Mexico, Apr. 1994.
- Invited Panelist on "Will Massively Parallel Processing be General Purpose" at IPPS-93 conference, NewPort Beach, Apr. 1993.
- Invited Panelist on "Is Parallel Processing for CAD Real?" at CANDE Workshop, Mar. 1992.
- Panel member, National Science Foundation Panel on Reviewing SBIR Proposals, 1989.

- Session Chairs of various conferences: Int. Parallel Processing Symp (IPPS), 1994, 1993, 1991, Int. Conf. on Computer-Aided Design (ICCAD), 1990, Int. Conf. on Parallel Processing (ICPP), 1994, 1993, 1990, 1988.
- Presented Invited Presentations at Caltech, UCLA, IBM, Texas Instruments, Jet Propulsion Lab, Westinghouse, General Electric, UTexas, Stanford, UIowa, Univ. Minnesota, MIT, Princeton, Univ. Washington, Purdue, Georgia Tech, Northwestern, UC Berkeley.
- Consultant to Westinghouse Corporation, Jet Propulsion Laboratory, Research Triangle Institute, General Electric, United Nations Development Program, AT&T, Integrated Computing Engines, Ambit Design Systems, Atrenta, MediaworksSOC, Calypto Design Systems.

## RECENT INVITED LECTURES

- “Compiling Software Binary Programs onto Hardware,” Invited Lecture, Intel Corporation, Santa Clara, CA, Dec.. 2003.
- “An Overview of a Compiler for Compiling MATLAB Programs onto FPGAs,” Invited Lecture, Imperial College, London, ENGLAND, July 2003.
- “An Overview of a Compiler for Compiling MATLAB Programs onto FPGAs,” Invited Lecture, University of Rome, Rome, ITALY, July 2003.
- Invited Speaker on “Overview of the FREEDOM Compiler for Compiling Assembly and Binary Programs onto FPGAs and ASICs.” Cadence Berkeley Labs, Apr. 2003.
- Invited Speaker on “Overview of the FREEDOM Compiler for Compiling Assembly and Binary Programs onto FPGAs and ASICs.” Xilinx, Apr. 2003.
- Invited Speaker on “Technology Commercialization and Entrepreneurship: A Case Study of Accelchip,” Northwestern University, Urbana, May 2003.
- Invited Speaker on “Technology Commercialization and Entrepreneurship: A Case Study of Accelchip,” University of Illinois, Urbana, Apr. 2003.
- Invited Speaker on “Overview of AccelChip” at Chicago Technology Forum, University of Chicago Business School, Oct. 2002.
- Invited Speaker on “Launching Products from a Startup Company: AccelChip,” at Northwestern University, ITEC Center, Oct. 2002.
- “An Overview of the AccelFPGA Compiler for Compiling MATLAB Programs onto FPGAs,” Invited Lecture, University of California, Berkeley, Nov. 2002.
- “An Overview of the AccelFPGA Compiler for Compiling MATLAB Programs onto FPGAs,” Indian Institute of Technology, Kharagpur, INDIA, Dec. 2001.
- “Overview of AccelChip” Invited Lecture at University of Illinois, Oct. 2001.
- Electrical and Computer Engineering Distinguished Lecturer, "MATCH: A MATLAB Compilation Environment for Adaptive Computing Systems," University of Toronto, Aug.. 2000.
- Computer and Information Science Distinguished Lecturer, "A MATLAB Compilation Environment for Adaptive Computing Systems," University of California, Irvine, June 2000.
- Electrical and Computer Engineering Outstanding Lecturer, "A MATLAB Compilation Environment for Adaptive Computing Systems," Illinois Institute of Technology, Apr. 2000.
- Electrical and Computer Engineering Distinguished Lecturer, "PROPERCAD: Parallel Algorithms for VLSI CAD" Texas A & M University, Mar. 2000.
- Electrical and Computer Engineering Distinguished Lecturer, "MATCH: A MATLAB Compilation Environment for Adaptive Computing Systems," Texas A & M University, Mar. 2000.
- Computer Science Distinguished Lecturer, "A MATLAB Compilation Environment for Adaptive Computing Systems," University of Florida, Gainesville, Jan. 1999.
- Keynote Speaker, "Recent Advances in Compilers for Distributed Memory Multicomputers," Int. Conf. on Parallel and Distributed Computing, New Orleans, LO, Oct. 1997.
- Keynote Speaker, "Compiling for Distributed Memory Multicomputers", Int. Workshop on Parallel Processing, Dec. 1994, Bangalore, INDIA.
- Keynote Speaker, "Parallel Algorithms for VLSI CAD", Parallel and Distributed CAD Workshop, part of Fifth Generation Computer Systems Conference, Tokyo, JAPAN, Dec. 1994.

- "A MATLAB Compilation Environment for Adaptive Computing Systems," Invited Lecture, Department of Electrical and Computer Engineering, University of Toronto, July 1998.
- Keynote Speaker, "Recent Advances in Compilers for Distributed Memory Multicomputers," Int. Conf. on Parallel and Distributed Computing, New Orleans, LO, Oct. 1997.
- "The PARADIGM Compiler for Distributed Memory Multicomputers," Invited Lecture, Department of Electrical and Computer Engineering, Indian Institute of Technology, Dec. 1997.
- "ProperCAD: Parallel Algorithms for VLSI CAD" Invited Lecture, Department of Electrical Engineering, University of California, Berkeley, July 1996.
- "The PARADIGM Compiler for Distributed Memory Multicomputers" Invited Lecture, Department of Computer Science, Stanford University, Mar. 1996.
- "The PARADIGM Compiler for Distributed Memory Multicomputers" Invited Lecture, Department of Computer Science, MIT, Oct. 1995.
- "ProperCAD: Parallel Algorithms for VLSI CAD" Invited Lecture, Department of Electrical Engineering, University of Texas at Austin, Aug. 1995.

#### **ADMINISTRATIVE EXPERIENCE:**

- Dean, College of Engineering, University of Illinois at Chicago
- Chairman, Electrical and Computer Engineering Department, Northwestern University, 1998 – 2001 and 2002-present
- Director, Center for Parallel and Distributed Computing, Northwestern University, 1996-present.
- Director, Computational Science and Engineering Program, 1994-96, University of Illinois at Urbana Champaign
- President and CEO, AccelChip, 2000-02

#### **MAJOR AREAS OF RESEARCH:**

1. Compilers for Adaptive Computing
2. Compilers for Low Power Computing
3. Compiling Software Binaries to Hardware.
4. Parallel Algorithms for VLSI Computer-Aided Design Applications
5. Parallelizing Compilers for Distributed Memory Multiprocessors

#### **TEACHING EXPERIENCE:**

- Started and taught the following courses at Northwestern University: Introduction to Parallel Computing (ECE C58) Advanced Digital Design (ECE C03) Parallel Algorithms for VLSI Computer-Aided Design (ECE D58)
- Taught the following courses at the University of Illinois: Introduction to VLSI Systems Design (ECE325) VLSI Design Projects (ECE326) Microcomputer Design Laboratory (ECE311) Design of Fault-Tolerant Digital Systems (ECE442) Introduction to Computer Engineering (ECE290). Parallel Algorithms for VLSI CAD (ECE 426). Introduction to Parallel Programming (ECE 392).
- Introduction to Parallel Programming, a 5-day short course at the Computational Material Science Summer School, University of Illinois, Aug. 1996.
- Introduction to Massively Parallel Processing, a 2-day short course at AT&T, July 1992, and June 1993.
- Massively Parallel Computing, a 2-day Satellite TV short course offered through National Technological University (NTU), April 1993.
- Fault Tolerant Multiprocessors, a 4 day short course at AT&T, Aug. 1993. Use of Parallel Processing for VLSI CAD, one-day tutorial at the IEEE Int. Conf. on Supercomputing, Washington, DC, 1992.
- Introduction to Massively Parallel Processing, a 2-day short course at the Du Page County professionals through the Continuing Education program of University of Illinois, Jun. 1992.
- Programming Parallel Processors, 2-week course arranged by United Nations Development Program at the Indian Institute of Science, Bangalore, INDIA, 1991, attended by 50 professionals in India.
- Fault Tolerant Computing, 16 week course at AT&T, Naperville, IL, Fall 1990, attended by 50 AT&T employees.

- Parallel Processing for VLSI CAD, one-day tutorial at the IEEE Int. Conf. on Computer-Aided Design, Santa Clara, CA, 1988, 100 professional attendees.
- Parallel Algorithms for VLSI CAD, one-day tutorial ACM/IEEE Design Automation Conference, Orlando, FL, 1990, 120 professional attendees.
- Parallel Algorithms for VLSI CAD, one-day tutorial Int. Parallel Processing Symp., Cancun, Mexico, Apr. 1994.

## **GRADUATE STUDENT SUPERVISION:**

### **Postdoctoral Student Supervised: 1**

1. B. Ramkumar, PROPERCAD: A Portable Object Oriented Parallel Environment for VLSI CAD, Jan. 1991-Aug. 1992.

### **Ph.D. Theses Supervised: 35**

1. A. L. N. Reddy, "Parallel Input/Output Architectures for Multiprocessors," CRHC-90-5, UILU-ENG-90-2235, UIUC Ph.D. Thesis, ECE Department, May 1990.

2. R. M. Kling "Optimization by Simulated Evolution and Its Application to Cell Placement," CRHC-90-7, UILU-ENG-90-2237, UIUC Ph.D. Thesis., ECE Department, May 1990.

3. S. Patil "Parallel Algorithms for Test Generation and Fault Simulation," CRHC-90-12, UILU-ENG-90-2245, UIUC Ph.D. Thesis, ECE Department, August 1990.

4. K. P. Belkhale "Parallel Algorithms for Computer-Aided Design with Applications to Circuit Extraction," CRHC-90-15, UILU-ENG-90-2252, UIUC Ph.D. Thesis, CS Department, August 1990.

5. V. Balasubramanian, "Analysis and Synthesis of Algorithm Based Error Detection in Multiprocessors," CRHC-91-6, UIUC PhD Thesis, ECE Department, Feb. 1991.

6. R. Brouwer, "Parallel Algorithms for Placement and Routing," CRHC-91-2, UIUC PhD Thesis, ECE Department, Feb. 1991.

7. J. M. Hsu, "Performance Evaluation and Hardware Support of Message Communication in Distributed Memory Multicomputers," CRHC-91-5, UIUC PhD Thesis, CS Department, Feb. 1991.

8. M. Gupta, "Automated Data Partitioning in Distributed Memory Multicomputers," UIUC PhD Thesis, CS Department, September 1992.

9. S. Kim, "Novel Algorithms for Cell Placement and Their Parallel Implementations," UIUC PhD Thesis, ECE Department, July 1993.

10. K. De, "Parallel Algorithms for Logic Synthesis," UIUC PhD Thesis, ECE Department, September 1993.

11. S. Parkes, "A Class Library Approach to Concurrent Object-Oriented Programming with Applications to VLSI CAD," UIUC Ph.D. Thesis, ECE Department, September 1994.

12. M. Peercy, "Design of Hardware and Software Reconfiguration Strategies for Distributed Memory Multicomputers," UIUC Ph.D Thesis, ECE Department, September 1994.

13. A. Lain, "Compiler and Runtime System for Supporting Irregular Applications in Distributed Memory Multicomputers," UIUC Ph.D. Thesis, CS Department, October 1995.

14. A. Roy-Chowdhury, "Manual and Compiler Assisted Techniques for Synthesizing Fault-Tolerant Parallel Programs," UIUC Ph.D. Thesis, ECE Department, November 1995.

15. S. Ramaswamy, "Simultaneous Exploitation of Task and Data Parallelism in Regular Scientific Applications," UIUC Ph.D. Thesis, ECE Department, January 1996.
16. D. Palermo, "Compiler Techniques for Optimizing Communication and Data Distribution in Distributed Memory Multicomputers," UIUC Ph.D. Thesis, ECE department, May 1996.
17. J. Chandy, "Parallel Algorithms for Standard Cell Placement Using Simulated Annealing," UIUC Ph.D. Thesis, ECE department, July 1996.
18. E. Su, "A Compilation Framework for Distributed Memory Message-Passing Multicomputers," UIUC Ph.D. Thesis, ECE department, Mar. 1997.
19. J. Holm, "Performance Evaluation of Message-Driven Parallel Applications on General-Purpose Multiprocessors," UIUC Ph.D. Thesis, ECE department, Apr. 1997.
20. V. Krishnaswamy, "Parallel Algorithms for VHDL Simulation," UIUC Ph.D. Thesis, CS department, Apr. 1997.
21. Z. Xing, Novel Algorithms for Placement and Routing and their Parallel Implementations, UIUC Ph.D. Thesis, CS department, Jul. 1997.
22. D. Krishnaswamy, "Parallel Algorithms for Test Generation and Fault Simulation," UIUC Ph.D. Thesis, ECE department, Jul. 1997.
23. G. Hasteer, "Equivalence Checking in a Modular Checking Framework," UIUC Ph.D. Thesis, CS department, Dec. 1997.
24. S. Roy, "Low Power Driven Sequential Algorithms for Combinational and Sequential Circuits," UIUC Ph.D. Thesis, ECE Department, Aug. 1998.
25. P. Prabhakaran, "Improved Algorithms for High-Level Synthesis and Their Parallel Implementations," UIUC Ph.D. Thesis, CS department, Oct. 1998.
26. D. Chakrabarti, "Design and Evaluation of a Uniform Compilation Framework for Hybrid Applications," Northwestern Univ. ECE Department, June 2000.
27. Y. Yuan, "Novel Algorithms for 3-D Capacitance Extraction and the Parallel Implementations," Northwestern Univ. ECE Department, June 2000.
28. M. Haldar, "Optimized Hardware Synthesis for FPGAs," Northwestern University, ECE Department, Aug. 2001.
29. A. Nayak, "Automatic Parallelization and Optimizations for Synthesizing MATLAB Programs on Multi FPGA Systems," Northwestern University, ECE Department, Aug. 2001.
30. A. K. Jones, "PACT HDL: A C Compiler with Power and Performance Optimizations," Northwestern University, ECE Department, Aug. 2002.
31. Pramod Joisha, "A Type Inferencing System for MATLAB," Northwestern University, ECE Department, Aug. 2003.
32. Xiaoyong Tang, "High-Level Synthesis Algorithms for Low Power ASIC Design," Northwestern University, ECE Department, June 2004.
33. Tianyi Jiang, "Power Aware High-level Synthesis Techniques for FPGAs," Northwestern University, ECE Department, June 2004.

34. Gaurav Mittal, "A Compiler Infrastructure for Compiling Assembly and Binary Programs onto Field Programmable Gate Arrays." Northwestern University, ECE Department, August 2004.

35. David Zaretsky, "A Methodology for Mapping Scheduled Software Binaries onto Field Programmable Gate Arrays." Northwestern University, ECE Department, September 2005.

#### **M.S. Theses Supervised: 40**

A. Dugar (1986), R. M. Kling (1987), A. L. N. Reddy (1987), V. Balasubramanian (1987), M. Jones (1987), R. Brouwer (1988), A. Hagin (1988), K. P. Belkhale (1988), J. Sargent (1988), M. Peercy (1989), S. Kim (1989), H. Rao (1989), K. De (1990), G. Zipfel (1991), C. F. Lim (1991), A. Roy Chowdhury (1992), J. Chandy (1992), E. Su (1993), K. McPherson (1995), E. W. Hodges (1995), A. Mishra (1995), G. Hasteer (1995), S. Roy (1996), V. Kim (1998), P. Joisha (1998), A. Ye (1999), S. Periyacheri (1999), C. Bachmann (1999), A. Nayak (1999), M. Haldar (1999), A. Jones (2000), D. Zaretsky (2001), M. Walkden (2001), S. Pal (2001), D. Bagchi (2001), N. Tripathi (2001), N. Liveris (2003), R. Mukherjee (2003), S. Roy (2003), A. Malik (2004).

#### **COMPANIES WHERE FORMER Ph.D. STUDENTS ARE WORKING:**

- R. M. Kling, Intel
- S. Patil, went to IBM, now at Mentor Graphics
- K. P. Belkhale, went to IBM, now at Cadence Design Systems
- J. M. Hsu, Hewlett Packard
- M. Gupta, IBM
- S. Kim, went to LSI Logic, now at Synopsys
- K. De, went to LSI Logic, now at Cadence
- S. Parkes, started own company, Sierra Vista Research, now at IBM Almaden
- M. Peercy, IBM
- A. Lain, Hewlett-Packard
- A. Roy-Choudhary, Transarc Corporation
- S. Ramaswamy, IBM
- D. Palermo, Hewlett Packard
- E. Su, Intel
- J. Holm, Intel
- Z. Zhing, Sun
- V. Krishnaswamy, went to Intel, now at Calypto Design Systems
- D. Krishnaswamy, went to Intel, now at Calypto Design Systems
- G. Hasteer, Cadence Design Systems
- S. Roy, Cadence Design Systems
- P. Prabhakaran, Compaq-Digital
- D. Chakrabarti, Hewlett-Packard
- Y. Yuan, Synopsys
- M. Haldar, went to AccelChip, now at Calypto Design Systems.
- A. Nayak, went to AccelChip, now at Atrenta, Inc.
- P. G. Joisha, Microsoft Research
- X. Tang, Magma Design Automation
- T. Jiang, Marvel
- G. Mittal, BINACHIP
- D. Zaretsky, BINACHIP

#### **UNIVERSITIES WHERE FORMER Ph.D. STUDENTS ARE WORKING:**

- A. L. N. Reddy, Texas A & M University, Texas.
- R. Brouwer, Calvin College, Michigan.

- V. Balasubramian, Xavier University, Louisiana.
- Amitabh Mishra, Virginia Tech
- J. Chandy, University of Connecticut
- A. K. Jones, University of Pittsburg

## TOP 10 MOST CITED PUBLICATIONS ON GOOGLE SCHOLAR 12/23/2005

1. [Demonstration of automatic data partitioning techniques for parallelizing compilers on](#) - [Full-Text @ My Library](#)  
M Gupta, **P Banerjee** - IEEE Transactions on Parallel and Distributed Systems, 1992 - [ece.nwu.edu](#)  
[Cited by 183](#) - [View as HTML](#) - [Web Search](#) - [research.ibm.com](#) - [ece.northwestern.edu](#) - [crhc.uiuc.edu](#) - [all 9 versions](#)
2. [An Overview of the PARADIGM Compiler for Distributed-Memory Multicomputers](#)  
**P Banerjee**, JA Chandy, M Gupta, EW Hodges IV, JG - IEEE Computer, 1995 - [ece.nwu.edu](#)  
[Cited by 126](#) - [View as HTML](#) - [Web Search](#) - [research.ibm.com](#) - [crhc.uiuc.edu](#) - [scarpaz.com](#) - [all 12 versions](#)
3. [Parallel algorithms for VLSI computer-aided design applications](#)  
**P Banerjee** - 1994 - Englewood Cliffs, NJ: Prentice-Hall  
[Cited by 80](#) - [Web Search](#) - [Library Search](#)
4. [An Evaluation of Multiple-Disk I/O Systems](#) - [Full-Text @ My Library](#)  
ALN Reddy, **P Banerjee** - IEEE Transactions on Computers, 1989 - [portal.acm.org](#)  
[Cited by 61](#) - [Web Search](#) - [dx.doi.org](#) - [ieeexplore.ieee.org](#) - [csa.com](#) - [all 5 versions](#)
5. [CHIMAERA: a high-performance architecture with a tightly-coupled reconfigurable functional unit](#)  
ZA Ye, A Moshovos, S Hauck, **P Banerjee** - CONF PROC ANNU INT SYMP COMPUT ARCHIT ISCA. pp. 225-235. , 2000 - [portal.acm.org](#)  
[Cited by 68](#) - [Web Search](#) - [doi.ieeecomputersociety.org](#) - [crhc.uiuc.edu](#) - [users.ece.gatech.edu](#) - [all 20 versions](#) - [Resources @ My Library](#)
6. [Automatic generation of efficient array redistribution routines for distributed memory](#)  
S RAMASWAMY, **P BANERJEE** - 1994 - [crhc.uiuc.edu](#)  
[Cited by 61](#) - [View as HTML](#) - [Web Search](#) - [zikova.cvut.cz](#) - [ece.northwestern.edu](#) - [ece.nwu.edu](#) - [all 12 versions](#)
7. [Improving locality using loop and data transformations in an integrated framework](#)  
M Kandemir, A Choudhary, J Ramanujam, **P Banerjee** - PROC ANNU INT SYMP MICROARCHITECTURE. pp. 285-296. 1998, 1998 - [ieeexplore.ieee.org](#)  
[Cited by 62](#) - [Web Search](#) - [doi.ieeeecs.org](#) - [doi.ieeecomputersociety.org](#) - [portal.acm.org](#) - [all 7 versions](#) - [Resources @ My Library](#)
8. [A MATLAB Compiler for Distributed, Heterogeneous, Reconfigurable Computing Systems](#)  
**P Banerjee**, N Shenoy, A Choudhary, S Hauck, C - Proc. IEEE Symposium on FPGA as Custom Computing Machines, , 2000 - [doi.ieeecomputersociety.org](#)  
[Cited by 51](#) - [Web Search](#) - [doi.ieeeecs.org](#) - [ece.northwestern.edu](#) - [ece.nwu.edu](#) - [all 12 versions](#) - [Resources @ My Library](#)
9. [Parallel simulated annealing algorithms for cell placement on hypercube multiprocessors](#) - [Full-Text @ My Library](#)  
**P Banerjee**, MH Jones, JS Sargent - IEEE Transactions on Parallel and Distributed Systems, 1990 - [ieeexplore.ieee.org](#)  
Page 1 IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS, VOL. 1. NO. 1  
JANUARY 1990 91 1045-9219/90/OI00-0091\$01.00 1990 IEEE Parallel Simulated ...  
[Cited by 50](#) - [Web Search](#) - [doi.ieeeecs.org](#) - [doi.ieeecomputersociety.org](#) - [portal.acm.org](#) - [all 9 versions](#)
10. [Algorithm-based fault detection for signal processing applications](#) - [Full-Text @ My Library](#)  
ALN Reddy, **P Banerjee** - IEEE Transactions on Computers, 1990 - [portal.acm.org](#)  
[Cited by 42](#) - [Web Search](#) - [portal.acm.org](#) - [ieeexplore.ieee.org](#)

## COMPLETE LIST OF PUBLICATIONS

### BOOKS

1. P. Banerjee, *Parallel Algorithms for VLSI Computer-Aided Design*, Prentice-Hall, Inc., Englewoods-Cliffs, NJ, 1994.

### PATENTS

1. P. Banerjee, A. Choudhary, M. Haldar, A. Nayak, "Methods and Apparatus for Automatically Generating Hardware from Algorithms Described in MATLAB." US Patent Number 7,000,213, granted Feb. 14, 2006.
2. P. Joisha, P. Banerjee, N. Shenoy, "Method for Array Shape Inferencing for a Class of Functions in MATLAB," US Patent Number 7,086,040, granted Aug. 1, 2006.

### CHAPTERS IN BOOKS

1. P. Banerjee, M. Jones, J. Sargent, R. Brouwer, K. P. Belkhale, and S. Patil, "Parallel Algorithms for VLSI Computer-Aided Design Toolson Hypercube Multiprocessors," in *Advances in Computer-Aided Design*, Editor: I. N. Hajj, JAI Press, England, Volume 2, 1990.
2. P. Banerjee, "HIPERCAD: Parallel Algorithms for High Performance VLSI CAD", in *VLSI System Design*, Editors: Patnaik and Singh, Tata McGraw Hill Publishing Co., New Delhi, INDIA, pp. 27-33, 1990.
3. R. K. Iyer, J. H. Patel, W. K. Fuchs, P. Banerjee, R. Horst, "Hardware and Software Fault Tolerance," *Encyclopedia of Microcomputers*, Marcel Dekker, 1991.
4. P. Banerjee, "A Survey of Parallel Algorithms for VLSI Cell Placement," *Lecture Notes in Computing*, Special Issue on Algorithmic Aspects of VLSI Layout, Springer Verlag, Wien, New York, January, 1993.
5. D. K. Pradhan and P. Banerjee, "Fault Tolerant Multiprocessor and Distributed Systems: Principles," chapter in *Fault Tolerant System Design*, Editor: D. Pradhan, Prentice-Hall, Englewoods Cliffs, NJ, 1996.
6. P. Banerjee, V. Balasubramanian, and A. Roy Chowdhury, "Compiler Assisted Synthesis of Algorithm Based Checking in Multiprocessors," chapter in *Foundations of Ultradependable Computing*, Volume III: System Implementations Editors: G. M. Koob, C. Lau, Kluwer Academic Publishers, Norwell, MA, 1994.
7. D. J. Palermo, E. W. Hodges, and P. Banerjee, "Dynamic Data Partitioning for Distributed Memory Multicomputers," chapter in *Languages, Compilation Techniques, and Runtime Systems for Scalable Parallel Systems (Recent Advances and Future Perspectives)* Editors: S. Pande and D. P. Agarwal, Springer Verlag Publishers, 1997.
8. S. Mohan, P. Mazumder, D. Krishnaswamy, P. Banerjee, and E. M. Rudnick, "Parallel Implementations," chapter in *Genetic Algorithms for VLSI Design, Layout & Test Automation*, Editors: P. Mazumder and E. M. Rudnick, Prentice Hall PTR, 1999.
9. M. Kandemir, J. Ramanujam, A. Choudhary, and P. Banerjee, "An Iteration Space Transformation Algorithm Based on Explicit Data Layout Representation for Optimizing Locality," in *Languages and Compilers for Parallel Computers*, Editors: S. Chatterjee et al., *Lecture Notes in Computer Science*, Springer-Verlag, 1999.
10. A. Jones, D. Bagchi, S. Pal, A. Choudhary, and P. Banerjee, "PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations," in *Power Aware Computing*, Editors: R. Melhem and Bob Graybill, Kluwer Academic Publishers, 2001.

## ARTICLES IN JOURNALS

1. P. Banerjee and J. A. Abraham, "Characterization and Testing of Physical Failures in MOS Logic Circuits," *IEEE Design and Test*, Aug. 1984, pp. 76-86.
2. P. Banerjee and J. A. Abraham, "A Multi-valued Algebra for Modeling Physical Failures in MOS VLSI Circuits," *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, Vol. CAD, no. 3, Jul. 1985, pp. 312-321.
3. P. Banerjee and J. A. Abraham, "Bounds on Algorithm-Based Fault Tolerance in Multiple Processor Systems," *IEEE Transactions Computers*, Vol. C-35, no. 4, Apr. 1986, pp. 296-306.
4. J. A. Abraham, P. Banerjee, C.-Y. Chen, W. K. Fuchs, S.-Y. Kuo, and A. L. N. Reddy, "Fault tolerance techniques for systolic arrays," *IEEE Computer*, Vol. 20, no. 7, Jul. 1987, pp. 65-77.
5. V. Balasubramanian and P. Banerjee, "A Fault Tolerant Massively Parallel Processing Architecture," *Journal of Distributed and Parallel Computing*, Aug. 1987, pp. 363-383.
6. P. Banerjee, "The Cubical Ring-Connected Cycles: A Fault Tolerant Parallel Computation Network," *IEEE Trans. Computers*, Vol. C-37, No. 5, May 1988, pp. 632-636.
7. D. B. West and P. Banerjee, "On The Construction of Communication Networks Satisfying Bounded Fan-in of Service Ports," *IEEE Trans. Computers*, Vol. C-37, No. 9, Sep. 1988, pp. 1148-1151.
8. P. Banerjee and A. Dugar, "Design, Analysis, and Simulation of a Fault-Tolerant Interconnection Network supporting the Fetch-Add Primitive," *IEEE Trans. Computers*, Vol C-38, No. 1, Jan. 1989, pp. 30-46.
9. R. M. Kling and P. Banerjee, "ESP: Placement by Simulated Evolution," *IEEE Trans. Computer-Aided Design of Circuits and Systems*, Vol. CAD-8, no. 3, Mar. 1989, pp. 245-256.
10. A. L. N. Reddy and P. Banerjee, "An Evaluation of Multiple-Disk I/O Systems," *IEEE Trans. Computers*, Vol. 38, no. 12, Dec. 1989, pp. 1680-1690.
11. P. Banerjee, M. H. Jones, and J. S. Sargent, "Parallel Simulated Annealing Algorithms for Standard Cell Placement on Hypercube Multiprocessors," *IEEE Trans. Parallel and Distributed Systems*, Vol. 1, no. 1, Jan. 1990, pp. 91-106.
12. V. Balasubramanian and P. Banerjee, "Trade-offs in the Design of Efficient Algorithm-Based Error Detection Schemes for Hypercube Multiprocessors," *IEEE Trans. Software Engineering*, Vol. 16, no. 2, Feb. 1990, pp. 183-195.
13. S. Patil and P. Banerjee, "A Parallel Branch and Bound Algorithms for Test Generation," *IEEE Trans. Computer-Aided Design of Circuits and Systems*, Vol. 9, no. 3, Mar. 1990, pp. 313-322.
14. A. L. N. Reddy and P. Banerjee, "Design, Analysis and Simulation of I/O Architectures for Hypercube Multiprocessors," *IEEE Trans. Parallel and Distributed Systems*, Vol. 1, no. 2, Apr. 1990, pp. 140-151.
15. V. Balasubramanian and P. Banerjee, "Compiler Assisted Algorithm-Based Checking for Multiprocessors," *IEEE Trans. Computers*, Apr. 1990, Vol. 39, no. 4, pp. 436-447.
16. P. Banerjee, J. T. Rahmeh, C. B. Stunkel, V. S. S. Nair, K. Roy, J. A. Abraham, and V. Balasubramanian, "Algorithm Based Fault Tolerance on Hypercube Multiprocessors," *IEEE Trans. Computers*, Vol. 39, No.9, pp 1132-1142, Sep. 1990.
17. A. L. N. Reddy and P. Banerjee, "Algorithm-Based Fault Detection in Signal Processing Applications," *IEEE Trans. Computers*, Vol. 39, No. 10, pp. 1304-1308, Oct. 1990.

18. K. P. Belkhale and P. Banerjee, "Reconfiguration Strategies for VLSI Processor Arrays and Trees Using a Modified Diogenes Approach" IEEE Trans. Computers, Jan. 1992.
19. K. P. Belkhale and P. Banerjee "Parallel Algorithms for VLSI Circuit Extraction" IEEE Trans. Computer Aided Design, Vol. 10, No. 5, pp. 604-618, May 1991.
20. S. Patil and P. Banerjee, "Performance Trade-offs in a Parallel Test Generation Fault Simulation Environment," IEEE Trans. Computer-Aided Design, Vol. 10, No. 12, Dec. 1991, pp. 1542-1558.
21. R. M. Kling and P. Banerjee, "Empirical and Theoretical Studies of the Simulated Evolution Method Applied to Standard Cell Placement," IEEE Trans. Computer-Aided Design, Oct. 1991, Vol. 10, no. 10, pp. 1303-1315.
22. M. Gupta and P. Banerjee, "Demonstration of Automated Data Partitioning Techniques in Parallelizing Compilers for Distributed Memory Multiprocessors," IEEE Trans. Parallel and Distributed Systems, March, 1992, Vol. 3, no. 2, pp. 179-193.
23. J.-M. Hsu and P. Banerjee, "Performance Measurement and Trace Driven Simulation of Parallel CAD and Numeric Applications on a Hypercube Multicomputer," IEEE Trans. Parallel and Distributed Systems, July 1992, Vol. 3, No. 3, pp. 451-464.
24. K. P. Belkhale and P. Banerjee, "Parallel Algorithms for Geometric Connected Labeling on Hypercube Multiprocessors," IEEE Trans. Computers, Vol. 41, No. 6, Jun. 1992, pp. 699-709.
25. A. L. N. Reddy, J. Chandy, and P. Banerjee, "Design and Evaluation of Gracefully Degraded Disk Arrays," Journal of Parallel and Distributed Computing, Jan. 1993.
26. M. Peercy and P. Banerjee, "Fault Tolerant VLSI Systems," Proceedings of the IEEE (Special Issue on VLSI Reliability), (invited paper), May 1993, Volume 81, number 5, pp. 745-758.
27. K. P. Belkhale and P. Banerjee, "Task Scheduling for Exploiting Parallelism and Hierarchy in VLSI CAD Applications," IEEE Trans. Computer-Aided Design, Volume 12, number 5, May 1993, pp. 557-567.
28. K. De and P. Banerjee, "PREST: A System for Logic Partitioning and Resynthesis," IEEE Trans. On VLSI Systems, Vol. 1, no. 4, pp. 514-525, December 1993.
29. K. De, B. Ramkumar and P. Banerjee, "A Portable Parallel Algorithm for Logic Synthesis using Transduction," IEEE Trans. Computer-Aided Design, Volume 13, number 5, May 1994, pp. 566-580.
30. P. Banerjee and M. Peercy, "Design and Evaluation of Hardware Reconfiguration Strategies for Hyper cubes and Meshes," IEEE Transactions on Computers, Volume 43, Number 7, July 1994, pp. 841-848.
31. K. De, C. Natarajan, D. Nair, and P. Banerjee, "RSYN: A System for Automated Synthesis of Reliable Multilevel Circuits," IEEE Transactions on VLSI Systems, Volume 2, number 2, June 1994, pp. 186-195.
32. B. Ramkumar and P. Banerjee, "ProperCAD: A Portable Object Oriented Parallel Environment for VLSI CAD," IEEE Transactions on Computer-Aided Design, Volume 13, Number 7, July 1994, pp. 829-842.
33. M. Gupta and P. Banerjee, "Compile-time Estimation of Communication Costs of Programs," Jour. Programming Languages, Vol. 2 (1994), pp. 191-225.
34. P. Banerjee, J. Chandy, M. Gupta, J. G. Holm, A. Lain, D. J. Palermo, S. Ramaswamy and E. Su, "The PARADIGM Compiler for Distributed Memory Multicomputers," IEEE Computer, Vol. 28, No. 10, Oct. 1995, pp. 37-47.

35. S. Ramaswamy and P. Banerjee, "Simultaneous Allocation and Scheduling Using Convex Programming Techniques," *Parallel Processing Letters (Special Issue on Partitioning and Scheduling)*, Dec. 1995.
36. A. Roy-Chowdhury and P. Banerjee, "A New Error Analysis Based Method for Tolerance Computation for Algorithm-Based Checks," *IEEE Trans. Computers*, Vol. 45, No. 2, Feb. 1996, pp. 238-243.
37. V. S. S. Nair, J. A. Abraham, P. Banerjee, "Efficient Techniques for the Analysis of Algorithm-Based Fault Tolerance (ABFT) Schemes" *IEEE Trans. Computers*, Vol. 45, No. 4, Apr. 1996, pp. 499-502.
38. A. Roy Chowdhury, N. Bellas, and P. Banerjee, "Algorithm-Based Error Detection Schemes for Iterative Solution of Partial Differential Equations," *IEEE Trans. Computers*, Vol. 45, No. 4, Apr 1996, pp 394-407.
39. A. Roy-Chowdhury and P. Banerjee, "Algorithm-based Fault Location and Recovery for Matrix Computations on Multiprocessor Systems," *IEEE Trans. Computers*, Vol. 45, no. 11, Nov. 1996, pp. 1239-1247.
40. E. Rudnick, V. Chickermane, P. Banerjee, J. H. Patel, "Sequential Circuit Testability Enhancement Using a Non-scan Approach," *IEEE Transactions on VLSI Systems*, 1996.
41. K. McPherson and P. Banerjee, "Parallel Algorithms for VLSI Layout Verification," *Journal of Parallel and Distributed Computing*, Vol. 36, No. 2, August 1996, pp. 156-172.
42. D. Palermo, E. W. Hodges and P. Banerjee, "Dynamic Data Partitioning for Distributed Memory Multicomputers," *Journal of Parallel and Distributed Computing (Special Issue on Compilation Techniques for Distributed Memory Systems)* November 1, 1996, Vol. 38, no. 2, pp. 158-175.
43. S. Ramaswamy, B. Simons and P. Banerjee, "Optimizations for Efficient Array Redistribution on Distributed Memory Multicomputers," *Journal of Parallel and Distributed Computing (Special Issue on Compilation Techniques for Distributed Memory Systems)* November 1, 1996, Vol. 38, no. 2, pp. 217- 228.
44. S. Ramaswamy, S. Sapatnekar, and P. Banerjee, "A Framework for Exploiting Data and Functional Parallelism on Distributed Memory Multicomputers," *IEEE Trans. Parallel and Distributed Systems*, Vol. 8, No. 11, pp. 1098-1116, November 1997.
45. B. Ramkumar and P. Banerjee, "ProperTEST: A Portable Parallel Test Generator for Sequential Circuits," *IEEE Trans. Computer-Aided Design*, Vol. 16, No. 5, pp. 555-569, May 1997.
46. G. Hasteer and P. Banerjee, "A Parallel Algorithm for State Assignment of Finite State Machines," *IEEE Transactions on Computers*, Vol. 47, No. 2, February 1998, pp. 242-246.
47. V. Krishnaswamy, R. Gupta and P. Banerjee, "Implications of VHDL Timing Models on Simulation and Software Synthesis," *Journal of Systems Architecture*, North-Holland Elsevier Publishers, Vol. 44, 1997, pp. 23-36.
48. G. Hasteer and P. Banerjee, "Simulated Annealing Based Parallel State Assignment for Finite State Machines," *Journal of Parallel and Dist. Computing*, Vol. 43, no. 1, May 25, 1997, pp. 21-35.
49. J. A. Chandy, S. Kim, B. Ramkumar, S. Parkes, and P. Banerjee "An Evaluation of Parallel Simulated Annealing Strategies with Applications to Standard Cell Placement", *IEEE Trans. on Computer Aided Design*, Vol. 16, No. 4, pp. 398-410, April 1997.
50. G. Hasteer, A. Mathur, and P. Banerjee, "Efficient Equivalence Checking of Multi-Phase Designs Using Phase Abstraction and Retiming.," *ACM Transactions on Design Automation of Electronic Systems (TODAES) Special Issue on High Level Design, Validation and Testing*, Oct. 1998, pp. 600-625.

51. M. Kandemir, A. Choudhary, N. Shenoy, P. Banerjee, J. Ramanujam, "A Linear Algebra Framework for Automatic Determination of Optimal Data Layouts," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 10, No. 2, February 1999, pp. 115-135.
52. J. Chandy and P. Banerjee, "A Parallel Circuit Partitioned Algorithm for Timing-Driven Standard Cell Placement," *Journal of Parallel and Distributed Computing*, vol. 57., No. 1, pp. 64-90, April 1999.
53. P. Prabhakaran and P. Banerjee, "Parallel Algorithms for Force-Directed Scheduling of Flattened and Hierarchical Signal Flow Graphs," *IEEE Transactions on Computers*, 1999.
54. M. Kandemir, P. Banerjee, A. Choudhary, J. Ramanujam, and N. Shenoy, "A Global Communication Optimization Technique Based on Data Flow Analysis and Linear Algebra," *ACM Trans. on Programming Languages and Systems (TOPLAS)*, Vol. 21, No. 6, Nov. 1999.
55. M. Kandemir, A. Choudhary, J. Ramanujam, and P. Banerjee, "A Matrix-Based Approach to Global Locality Optimization," *Journal of Parallel and Distributed Computing*, Special Issue on Compilation and Architectural Support for Parallel Applications, Vol. 58, No. 2, Aug. 1999, pp. 190-235.
56. A. Lain, D. Chakrabarti, and P. Banerjee, "Compiler and Run-Time Support for Exploiting Regularity Within Irregular Applications," *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 11, No. 2, February 2000.
57. M. Kandemir, N. Shenoy, P. Banerjee, J. Ramanujam, and A. Choudhary, "Minimizing Data and Synchronization Costs in One-Way Communication," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 11, No. 12, December 2000, pp. 1232-1251.
58. N. Shenoy, A. Choudhary, and P. Banerjee, "An Algorithm for Synthesis of Large Time-constrained Heterogeneous Adaptive Systems," *ACM Transactions on the Design Automation of Electronic Systems*, Vol. 6, No. 2, April 2001.
59. D. R. Chakrabarti and P. Banerjee, "Static Single Assignment Form for Message-Passing Programs," *International Journal of Parallel Programming*, to appear, 2001.
60. A. Nayak, M. Haldar, C. Chen, M. Sarrafzadeh, P. Banerjee, "Power Optimizations in Delay Constrained Circuits" *VLSI Design Journal* to appear, 2001.
61. P. Joisha and P. Banerjee, "The Efficient Computation of Ownership Sets in HPF," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 12, No. 8, August 2001.
62. M. Kandemir, P. Banerjee, A. Choudhary, J. Ramanujam, and E. Ayguade, "Static and Dynamic Locality Optimizations Using Integer Linear Programming," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 12, No. 9, pp. 922-941, September 2001.
63. Y. Yuan and P. Banerjee, "A Parallel Implementation of a Fast Multipole Based 3-D Capacitance Extraction Program on Distributed Memory Multicomputers," *Journal of Parallel and Distributed Computing*, Vol. 61, No. 12, December 2001, pp. 1751-1774.
64. V. Kim, P. Banerjee, K. De, and J. Brouwers, "Parallel and Distributed VLSI Synthesis on a Network of Workstations," *International Journal of Parallel and Distributed Systems and Networks*. to appear, 2001.
65. M. Kandemir, A. Choudhary, P. Banerjee, and J. Ramanujam, "Reducing False Sharing and Improving Spatial Locality in a Unified Compilation Framework," *IEEE Transactions on Parallel and Distributed Systems*, to appear.

66. M. Kandemir, J. Ramanujam, A. Choudhary, and P. Banerjee, "A Layout-Conscious Iteration Space Transformation Technique," *IEEE Transactions on Computers*, Vol. 50, No. 12, December 2001, pp. 1321-1336.
67. V. Krishnaswamy, G. Hasteer and P. Banerjee, "Automated Parallelization of Compiled Event Driven VHDL Simulation," *IEEE Transactions on Computers*, Vol. 51, No. 4, April 2002, pp. 380-394.
68. A. Mishra and P. Banerjee, "An Algorithm Based Error Detection Scheme for the Multigrid Method," *IEEE Transactions on Computers*, Vol. 52, No. 9, Sep. 2003, pp. 1089-1099.
69. P. Banerjee, V. Saxena, J. Uribe, M. Haldar, A. Nayak, V. Kim, S. Parkes, D. Bagchi, S. Pal, D. Zaretsky, N. Tripathi, B. Jiang, R. Anderson, T. Vanevenhoven, D. Nandy, "Overview of a Compiler for Synthesizing MATLAB Programs onto FPGAs," *IEEE Transactions on VLSI Systems*, Vol. 12, No. 4, April 2004.
70. T. Jiang, X. Tang, P. Banerjee, "Macro-models for high-level area and power estimation on FPGAs," to appear in special issue on *Mathematical Modeling and Simulation for Industrial Applications* of the *International Journal of Simulation and Process Modeling*, June 2005.
71. S. Roy and P. Banerjee, "An Algorithm for Trading off Quantization Error with Hardware Resources for MATLAB based FPGA Design," *IEEE Transactions on Computers*, July 2005, Vol. 54, No. 7, pp. 886-896.
72. P. Joisha and P. Banerjee, "An Algebraic Type Inference System for MATLAB", *ACM Transactions on Programming Languages and Systems (TOPLAS)*, to appear, 2006.
73. X. Tang, T. Jiang, A. K. Jones, and P. Banerjee, "High-Level Synthesis for Low Power Hardware Implementation of Unscheduled Data-Dominated Circuits," *Journal of Low Power Electronic (JOLE)*, American Scientific Publishers, to appear, 2006.
74. P. Joisha and P. Banerjee, "A Translator System for the MATLAB Language," *Software Practices and Experiences*, to appear, 2006
75. A. Mallik, D. Sinha, H. Zhou, and P. Banerjee, "Low Power Optimization by Smart Bit-width Allocation in a SystemC based ASIC Design Environment", *IEEE Transactions on Computer Aided Design of Integrated Circuits*, to appear, 2006.

## **PUBLICATIONS IN CONFERENCE PROCEEDINGS**

1. P. Banerjee and J. A. Abraham, "Fault Characterization of VLSI MOS Circuits," Proceedings, International Conference on Circuits and Computers, New York, NY, Sep. 1982, pp. 564-568.
2. P. Banerjee and J. A. Abraham, "MURPHY: A Logic Simulator for nMOS and CMOS VLSI Circuits," Proceedings, International Conference on Computer-Aided Design, Santa Clara, CA, Sep. 1983, pp. 94-95.
3. P. Banerjee and J. A. Abraham, "Generating Tests for Physical Failures in MOS Logic Circuits," Proceedings, International Test Conference, Cherry Hill, Philadelphia, Oct. 1983, pp. 554-559.
4. P. Banerjee and J. A. Abraham, "Fault-Secure Algorithms for Multiple-Processor Systems," Proceedings, 11th Annual International Symp. on Computer Architecture, Ann Arbor, MI, Jun. 1984, pp. 279-287.
5. D. B. West and P. Banerjee, "Partial Matching in Degree-Restricted Bipartite Graphs," Proc., Southeastern Intl. Conf. on Combinatorics, Graph Theory, and Computing, Congressus Numeratum, Boca Raton, FL, Feb. 1985, vol. 49, pp. 259-266.

6. P. Banerjee and J. A. Abraham,"Graph-Theoretic Bounds for On-Line Checks in Multiple Processor Systems,"Proceedings, AFIPS National Computer Conference, Las Vegas, NV, vol. 55, Jun. 1986, pp. 283-296.
7. P. Banerjee, S. Y. Kuo, and W. K. Fuchs,"Reconfigurable Cube-Connected Cycles Architectures,"Proceedings, 16th Annual Symposium on Fault-Tolerant Computing, Vienna, Austria, Jul. 1986, pp. 286-291.
8. P. Banerjee and J. A. Abraham,"Concurrent Fault Diagnosis in Multiple Processor Systems,"Proceedings 16th Annual Symposium on Fault-Tolerant Computing, Vienna, Austria, Jul. 1986, pp. 298-303.
9. A. Dugar and P. Banerjee,"A Fault-Tolerant Interconnection Network Supporting the Fetch-Add Primitive,"Proceedings, International Conference on Parallel Processing, St. Charles, IL, Aug. 1986, pp. 327-334.
10. V. Balasubramanian and P. Banerjee,"RECBAR: A Reconfigurable Massively Parallel Processing Architecture,"Proceedings, International Conference on Parallel Processing, St. Charles, IL, Aug. 1986, pp. 390-393.
11. R. M. Kling and P. Banerjee,"A Novel Circuit Design Providing Concurrent Error Detection in PLAs,"Proceedings, International Conference on Computer Design: VLSI in Computers, New York, NY, Oct. 1986, pp. 588- 591.
12. P. Banerjee and M. Jones,"A Parallel Simulated Annealing Algorithm for Standard Cell Placement on a Hypercube Computer,"Proceedings, International Conference on Computer-Aided Design, Santa Clara, CA, Nov. 1986, pp. 34-37.
13. P. Banerjee and J. A. Abraham,"A Probabilistic Model of Algorithm-Based Fault Detection and Tolerance in Array Processors for Real-Time Systems,"Proceedings, Real-Time Systems Symposium, New Orleans, LA, Dec. 1986, pp. 72-78.
14. A. L. N. Reddy and P. Banerjee,"A Fault-Secure Dictionary Machine,"Proceedings, Third International Conference on Data Engineering, Los Angeles, CA, Feb. 1987, pp. 104-109.
15. R. M. Kling and P. Banerjee, "ESP: A New Standard Cell Placement Package Using Simulated Evolution,"Proceedings, 24th Design Automation Conference, Miami Beach, FL, Jun. 1987, pp. 60-66.
16. M. Jones and P. Banerjee, "Performance of a Parallel Algorithm For Standard Cell Placement On The Intel Hypercube,"Proc. 24th Design Automation Conf., Miami Beach, FL, Jun. 1987, pp. 807-813.
17. B. Cunningham, W. K. Fuchs and P. Banerjee,"Fault Characterization and Delay Fault Testing of GaAs Logic Circuits,"Proc. Int. Test Conf., Washington, DC, Sep. 1987, pp. 836-842.
18. M. Jones and P. Banerjee,"An Improved Simulated Annealing Algorithm for Standard Cell Placement,"Proc. Int. Conf. on Computer Design, New York, NY, Oct. 1987, pp. 83-87.
19. R. M. Kling and P. Banerjee,"Concurrent ESP: A Placement Algorithm for Executive on Distributed Processors,"Proc. Int. Conf. on Computer-Aided Design (ICCAD-87), Santa Clara, CA, Nov. 1987, pp. 354-357.
20. V. Balasubramanian and P. Banerjee,"A Fixed Size Array Processor for Computing the Fast Fourier Transform," Proc. 8th IEEE Real-Time Systems Symp., San Jose, CA, Dec. 1987, pp. 36-43.
21. P. Banerjee,"Parallel Algorithms For VLSI CAD Tools on Hypercube Multiprocessors,"Proc. Int. Symp. on Electronic Devices, Circuits and Systems, Kharagpur, India, pp. 677-679, Dec. 1987.

22. P. Banerjee and C. Stunkel, "A Novel Approach to System-Level Fault Tolerance in Hypercube Multiprocessors," Proc. 3rd ACM Conference on Hypercube Concurrent Computers and Applications, Pasadena, CA, Jan. 1988, pp. 307-311.
23. P. Banerjee, J. T. Rahmeh, C. Stunkel, V. S. S. Nair, K. Roy, and J. A. Abraham, "An Evaluation of System-level Fault Tolerance on the Intel Hypercube Multiprocessor," Proc. 18th Int. Symp. Fault Tolerant Computing, Tokyo, Japan, 362-367, Jun. 1988.
24. A. L. N. Reddy, P. Banerjee, and S. G. Abraham, "I/O Embedding in Hypercubes," Proc. 17th Int. Conf. on Parallel Processing, Aug. 1988, St. Charles, IL, pp. 331-338.
25. R. Brouwer and P. Banerjee, "A Parallel Simulated Annealing Algorithm for Channel Routing on a Hypercube Multiprocessor," Proc. Int. Conf. on Computer-Design (ICCD-88), Oct. 1988, Rye Brook, NY, pp. 4-7.
26. K. P. Belkhale and P. Banerjee, "Reconfiguration Strategies in VLSI Processor Arrays," Proc. Int. Conf. on Computer-Design (ICCD-88), Oct. 1988, Rye Brook, NY, pp. 418-421.
27. K. P. Belkhale and P. Banerjee, "PACE: A Parallel VLSI Circuit Extractor on the Intel Hypercube Multiprocessor," Proc. Int. Conf. on Computer-Aided Design, Santa Clara, CA, Nov. 1988, pp. 326-329.
28. P. Banerjee, "Reconfiguring a Hypercube Multiprocessor in the Presence of Faults," Proc. 4th ACM Conf. on Hypercube Concurrent Computers and Applications, Monterey, CA, Mar. 1989.
29. R. Kling and P. Banerjee, "A Special Purpose Coprocessor for Supporting Cell Placement and Floorplanning Algorithms," Proc. Custom Integrated Circuits Conf., San Diego, CA, May 1989.
30. A. L. N. Reddy and P. Banerjee, "I/O Issues for Hypercubes," Proc. 3rd Int. Conf. on Supercomputing, Athens, Greece, Jun. 1989.
31. S. Patil and P. Banerjee, "A Parallel Branch and Bound Algorithms for Test Generation," Proc. 26<sup>th</sup> Design Automation Conf., Las Vegas, NV, Jun. 1989, pp. 339-345.
32. J. Sargent and P. Banerjee, "A Parallel Row-Based Algorithm for Standard Cell Placement with Integrated Error Control," Proc. 26th Design Automation Conf., Las Vegas, NV, Jun. 1989, pp. 590-594.
33. R. B. Mueller-Thuns, D. McFarland and P. Banerjee, "Algorithm-Based Fault Tolerance for Adaptive Least Squares Lattice Filtering on a Hypercube Multiprocessor," Proc. Int. Conf. on Parallel Processing, St. Charles, IL, Aug. 1989, pp. 177-183.
34. A. L. N. Reddy and P. Banerjee, "Performance Evaluation of Multiple-Disk I/O Systems," Proc. Int. Conf. on Parallel Processing, St. Charles, IL, Aug. 1989, pp. 315-319.
35. S. Patil and P. Banerjee, "Fault Partitioning Issues in an Integrated Parallel Test Generation/Fault Simulation Environment," Proc. Int. Test Conf., Washington, DC, Sep. 1989, pp. 718-727.
36. S. Kim and P. Banerjee, "An Accurate Timing Model for Fault Simulation in MOS Circuits," Proc. Int. Conf. Computer-Aided Design, Santa Clara, CA, Nov. 1989, pp. 76-79.
37. K. P. Belkhale and P. Banerjee, "PACE2: An Improved Parallel VLSI Extractor with Parametric Extraction," Proc. Int. Conf. Computer-Aided Design, Santa Clara, CA, Nov. 1989, pp. 526-529.
38. S. Patil, P. Banerjee, and C. Polychronopolous, "Efficient Circuit Partitioning Algorithms for Parallel Logic Simulation," Proc. Supercomputing Conf., Reno, NV, Nov. 89, pp. 361-364.
39. V. Balasubramanian and P. Banerjee, "Algorithm based Error Detection for Signal Processing Application on a Hypercube Multiprocessor," Proc. 10th Int. Real-time Systems Symp., Los Angeles, CA, Dec. 1989.

40. K. P. Belkhale and P. Banerjee, "Recursive Partitions on Multiprocessors", Proc. 5th Distributed Memory Computing Conference, Charleston, SC, Apr. 1990.
41. M. Peercy and P. Banerjee, "A Method for Evaluating Message Communication in Faulty Hypercubes", Proc. 5th Distributed Memory Computing Conference, Charleston, South Carolina, Apr. 1990.
42. J.-M. Hsu and P. Banerjee, "Performance Measurement and Trace Driven Simulation of Parallel CAD and Numeric Applications on a Hypercube Multicomputer", Proc. 17th Int. Symp. Computer Architecture, Seattle, WA, May, 1990, pp. 260-269.
43. A.L.N. Reddy and P. Banerjee, "A Study of I/O Behavior of Perfect Benchmarks on a Multiprocessor", Proc. 17th Int. Symp. Computer Architecture, Seattle, WA, May, 1990, pp. 312-321.
44. R. J. Brouwer and P. Banerjee, "PHIGURE: A Parallel Hierarchical Global Router", Proc. 27th ACM/IEEE Design Automation Conf., Orlando, FL, Jun. 1990, pp. 360-364.
45. R.-M. Kling and P. Banerjee, "Optimization by Simulated Evolution with Application to Standard Cell Placement", Proc. 27th ACM/IEEE Design Automation Conf., Orlando, FL, Jun. 1990, pp. 20-25.
46. M. Peercy and P. Banerjee, "Distributed Algorithms for Shortest-Path, Deadlock-Free Routing and Broadcasting in Arbitrarily Faulty Hypercubes", Proc. 20th Int. Symp. on Fault-Tolerant Computing (FTCS20), Newcastle, England, Jun. 1990, pp. 218-225.
47. P. Banerjee, "Strategies for Reconfiguring Hypercubes Under Faults", Proc. 20th Int. Symp. on Fault Tolerant Computing (FTCS-20), Newcastle, England, Jun. 1990, pp. 210-215.
48. K. P. Belkhale and P. Banerjee, "Geometric Connected Component Labeling on Distributed Memory Multiprocessors", Proc. of Int. Conf. on Parallel Processing, St. Charles, IL, Aug. 1990, Vol. III, pp. 291-295.
49. J.-M. Hsu and P. Banerjee, "Hardware Support for Message Routing in a Distributed Memory Multicomputer", Proc. of Int. Conf. on Parallel Processing, St. Charles, IL, Aug. 1990, vol. I, pp. 508-515.
50. K. Belkhale and P. Banerjee, "Approximate Algorithms for the Partitionable Independent Task Scheduling Problem", Proc. of Int. Conf. on Parallel Processing, St. Charles, IL, Aug. 1990, Vol. I, pp. 72-75.
51. D. T. Blaauw, P. Banerjee, and J. A. Abraham, "Automatic Classification of Node Types in Switch-Level Descriptions", Proc. Int. Conf. on Computer Design (ICCD-90), Oct. 1990, Boston, MA.
52. D. T. Blaauw, R. B. Mueller-Thuns, D. G. Saab, P. Banerjee, and J. A. Abraham, "SNEL: A Switch level Simulator Using Multiple Levels of Functional Abstraction", Proc. Int. Conf. Compt. Aided Design (ICCAD-90), Nov. 1990, Santa Clara, CA.
53. K. P. Belkhale and P. Banerjee, "A Parallel Algorithm for Hierarchical Circuit Extraction", Proc. Int. Conf. Compt. Aided Design (ICCAD-90), Nov. 1990, Santa Clara, CA.
54. J. M. Hsu and P. Banerjee, "A Message Passing Coprocessor for Distributed Memory Multicomputers," Proc. ACM Supercomputing Conf., Nov. 1990, New York, NY.
55. K. De and P. Banerjee, "Can Test Length Be Reduced During Synthesis Process?," Int. VLSI Design Conf. (VLSI-91), New Delhi, India, Jan. 1991.
56. D. Blaauw, D. Saab, P. Banerjee, and J. A. Abraham, "Functional Abstraction of Logic Gates for Switch Level Simulation," Proc. European Design Automation Conf. (EDAC-91), Amsterdam, Netherlands, Mar. 1991.

57. K. P. Belkhale and P. Banerjee, "A Scheduling Algorithm for Parallelizable Dependent Tasks," Proc. 5<sup>th</sup> Int. Parallel Processing Symp. (IPPS-5), Los Angeles, CA, Apr. 1991.
58. M. Gupta and P. Banerjee, "Automated Data Partitioning on Distributed Memory Multiprocessors," Proc. 6th Distributed Memory Multicomputers Conference (DMMC6), Portland, OR, May 1991.
59. S. Patil and P. Banerjee, "Parallel Test Generation for Sequential Circuits on General Purpose Multiprocessors," Proc. 28th Design Automation Conf. (DAC-91), San Francisco, CA, Jun. 1991.
60. A. L. N. Reddy and P. Banerjee, "Gracefully Degradable Disk Arrays," Proc. 21st Fault Tolerant Computing Symp. (FTCS-21), Montreal, CANADA, Jul. 1991.
61. J. M. Hsu and P. Banerjee, "Performance Evaluation of Hardware Support for Message Passing in Distributed Memory Multicomputers," Proc. Int. Conf. Parallel Processing (ICPP-91), St. Charles, IL, Aug. 1991.
62. V. Balasubramanian and P. Banerjee, "CRAFT: Compiler-Assisted Algorithm-Based Fault Tolerance in Distributed Memory Multiprocessors," Proc. Int. Conf. Parallel Processing (ICPP-91), St. Charles, IL, Aug. 1991.
63. A. L. N. Reddy, P. Banerjee and D. K. Chen, "Compiler Support for Parallel I/O Operations," Proc. Int. Conf. Parallel Processing (ICPP-91), St. Charles, IL, Aug. 1991.
64. S. Kim, S. Patil and P. Banerjee, "A Layout Driven Design for Testability Technique for MOS VLSI Circuits," Proc. Int. Test Conf., Nashville, TN, Oct. 1991.
65. K. De and P. Banerjee, "Logic Partitioning and Resynthesis for Testability," Proc. Int. Test Conf., Nashville, TN, Oct. 1991.
66. R. Brouwer and P. Banerjee, "PARAGRAPH: A Parallel Algorithm for Simultaneous Placement and Routing Using Hierarchy," Proc. European Design Automation Conf. (EDAC-92), Brussels, Belgium, Mar. 1992.
67. M. Gupta and P. Banerjee, "Compile-Time Estimation of Communication Costs in Multicomputers," Proc. Int. Parallel Proc. Symp., Beverly Hills, CA, Mar. 1992.
68. K. De, C. Wu, and P. Banerjee, "Reliability Driven Logic Synthesis," Proc. Int. Conf. Circuits and Systems (ISCAS-92), San Diego, CA, May 1992.
69. S. Kim, P. Banerjee, C. Vivekanand, J. Patel, "APT: An Area-Performance-Testability Driven Placement Algorithm," Proc. 29th Design Automation Conf., Anaheim, CA., Jun. 1992.
70. M. Gupta and P. Banerjee, "A Methodology for High-Level Synthesis of Communication on Multicomputers," Proc. 6th ACM Int. Conf. Supercomputing (ICS-92), Jul. 1992, Washington, DC.
71. M. Peercy and P. Banerjee, "Design and Analysis of Software Reconfiguration Strategies of Hypercube Multiprocessors Under Multiple Faults," Proc. 22nd Fault Tolerant Computing Symp., Jul. 1992, Boston, MA.
72. B. Ramkumar and P. Banerjee, "ProperCAD: A Portable Object-Oriented Parallel Environment for VLSI CAD," Proc. Int. Conf. on Computer Design (ICCD-92), Boston, MA, Oct. 1992.
73. B. Ramkumar and P. Banerjee, "Portable Parallel Test Generation for Sequential Circuits," Proc. Int. Conf. on Computer-Aided Design (ICCAD-92), Santa Clara, CA, Nov. 1992.
74. K. De, B. Ramkumar and P. Banerjee, "ProperSYN: A Portable Parallel Algorithm for Logic Synthesis," Proc. Int. Conf. on Computer-Aided Design (ICCAD-92), Santa Clara, CA, Nov. 1992.

75. J. G. Holm and P. Banerjee, "Low Cost Concurrent Error Detection in a VLIW Architecture Using Replicated Instructions," Proc. Int. Conf. Parallel Processing (ICPP-92), St. Charles, IL, Aug. 1992, Volume I, pp. 192-195.
76. C. F. Lim, P. Banerjee, K. De, and S. Muroga, "A Shared Memory Parallel Algorithm for Logic Synthesis," Proc. 6th Int. Conf. VLSI Design, Bombay, INDIA, Jan. 1993.
77. B. Ramkumar and P. Banerjee, "A Portable Parallel Algorithm for VLSI Circuit Extraction", Proc. Int. Parallel Processing Symp. (IPPS-93), Newport Beach, CA, Apr. 1993.
78. V. Chickermane, E. Rudnik, P. Banerjee, and J. Patel, "Nonscan Design for Testability Techniques for Sequential Circuits," Proc. Design Automation Conf. (DAC-93), Dallas, TX, Jun. 1993.
79. A. Roy Chowdhury and P. Banerjee, "Tolerance Determination for Algorithm-based Checks Using Simplified Error Analysis," Proc. Fault-Tolerant Computing Symposium (FTCS-93), Toulouse, FRANCE, Jun. 1993.
80. M. Gupta and P. Banerjee, "PARADIGM: A Compiler for Automated Data Partitioning", Proc. Int. Conf. Supercomputing (ICS-93), Tokyo, JAPAN, Jul. 1993.
81. S. Ramaswamy and P. Banerjee, "Processor Allocation and Scheduling of Macro Dataflow Graphs on Distributed Memory Multicomputers by the PARADIGM Compiler", Proc. Int. Conf. Parallel Processing (ICPP-93), St. Charles, IL, Aug. 1993.
82. J. Chandy and P. Banerjee, "Reliability Evaluation of Disk Array Architectures," Proc. Int. Conf. Parallel Processing (ICPP-93), St. Charles, IL, Aug. 1993.
83. A. Roy Chowdhury and P. Banerjee, "A Fault Tolerant Parallel Algorithm for Iterative Solution of the Laplace Equation," Proc. Int. Conf. Parallel Processing (ICPP-93), St. Charles, IL, Aug. 1993.
84. E. Su, D. Palermo, and P. Banerjee, "Automatic Parallelization of Regular Computations for Distributed Memory Multicomputers in the PARADIGM Compiler," Proc. Int. Conf. Parallel Processing (ICPP-93), St. Charles, IL, Aug. 1993.
85. S. Kim, J. Chandy, B. Ramkumar, S. Parkes, and P. Banerjee, "ProperPLACE: A Portable, Parallel Algorithm for Standard Cell Placement," Proc. 8th Int. Parallel Processing Symp., Cancun, Mexico, April 1994, pp. 932-941.
86. J. Holm, A. Lain, and P. Banerjee, "Compilation of Scientific Programs into Multithreaded and Message Driven Computation," Proc. Scalable High Performance Computing Conf., Knoxville, TN, May 1994, pp. 519-524.
87. S. Parkes, P. Banerjee, and J. Patel, "ProperHITEC: A Portable, Parallel, Object-Oriented Approach to Sequential Test Generation", Proc. 31st Design Automation Conf., San Diego, CA, June 1994, pp. 717-721.
88. A. Roy Chowdhury and P. Banerjee, "Algorithm-based Fault Location and Recovery for Matrix Computations," Proc. Fault Tolerant Computing Symp., Austin, TX, July 1994, pp. 38-48.
89. T. Karnik, S. Ramaswamy, S. M. Kang, and P. Banerjee, "Application of Algorithm Based Fault Tolerance Techniques to High Level Synthesis of Signal Flow Graphs," Proc. SPIE Int. Symp. Advanced Signal Processing Algorithms Architectures Implementations V, San Diego, CA, July 1994, pp. 760-776.
90. A. Lain and P. Banerjee, "Techniques to Overlap Computation and Communication in Irregular Iterative Applications," Proc. Int. Conf. Supercomputing, Manchester, England, July 1994, pp. 236-245.

91. E. Su, D. Palermo, and P. Banerjee, "Processor Tagged Descriptors: A Data Structure for Compiling for Distributed Memory Multicomputers," Proc. Conf. Parallel Architectures Compilation Techniques, Montreal, Canada, Aug. 1994, pp. 123-134.
92. D. Palermo, E. Su, and P. Banerjee, "Communication Optimizations Used in the PARADIGM Compiler for Distributed Memory Multicomputers," Proc. Int. Conf. Parallel Processing, St. Charles, IL, Aug. 1994, Vol II-1-11. THIS PAPER RECEIVED THE OUTSTANDING PAPER AWARD AT ICPP-94.
93. K. De and P. Banerjee, "Parallel Logic Synthesis Using Partitioning," Proc. Int. Conf. Parallel Processing, St. Charles, IL, Aug. 1994, Vol. III-135-141.
94. S. Ramaswamy, S. Sapatnekar, and P. Banerjee, "A Convex Programming Approach for Exploiting Data and Functional Parallelism on Distributed Memory Multicomputers," Proc. Int. Conf. Parallel Processing, St. Charles, IL, Aug. 1994, Vol. II-116-125.
95. S. Parkes, J. Chandy, and P. Banerjee, "A Library-Based Approach to Portable, Parallel, Object-Oriented Programming: Interface, Implementation, and Application," Proc. ACM Supercomputing 94 Conf., Washington, DC, Nov. 1994, pp. 69-78.
96. P. Banerjee, J. Chandy, M. Gupta, J. G. Holm, A. Lain, D. J. Palermo, S. Ramaswamy and E. Su, "The PARADIGM Compiler for Distributed Memory Message-Passing Multicomputers," Proc. First Int. Workshop on Parallel Processing, Bangalore, INDIA, Dec. 1994, pp. 322-330.
97. P. Banerjee, "A Survey of Current and Future Research Directions in Parallel CAD", Proc. Parallel and Distributed LSI-CAD Workshop, Tokyo, JAPAN, Dec. 1994, pp. 57-66.
98. S. Ramaswamy and P. Banerjee, "Automatic Generation of Efficient Array Redistribution Routines for Distributed Memory Multicomputers," Proc. 5th Symp. Frontiers of Massively Parallel Computation', McLean, VA, Feb. 1995, pp. 342-349.
99. A. Lain and P. Banerjee, "Exploiting Spatial Regularity with Irregular Iterative Applications," Proc. 8<sup>th</sup> Int. Parallel Processing Symp (IPPS-95), Santa Barbara, CA, Apr. 1995.
100. K. De, J. Chandy, S. Roy, S. Parkes and P. Banerjee, "Parallel Algorithms for Logic Synthesis Based on MIS" Proc. 8th Int. Parallel Processing Symp (IPPS-95), Santa Barbara, CA, Apr. 1995.
101. M. Peercy and P. Banerjee, "Software Schemes of Reconfiguration and Recovery in Distributed Memory Multicomputers Using the Actor Model" Proc. Fault Tolerant Computing Symp. (FTCS-25), Jun. 1995, Pasadena, CA.
102. D. Palermo and P. Banerjee, "Automatic Selection of Dynamic Data Partitioning Schemes for Distributed Memory Multicomputers," Proc. 8th Int. Workshop on Languages and Compilers for Parallel Computing (LCPC95, Aug. 1995, Columbus, OH.
103. S. Parkes, P. Banerjee and J. H. Patel, "A Parallel Algorithm for Fault Simulation Based on PROOFS," Int. Conf. Computer Design (ICCD 95), Austin, TX, Oct. 1995.
104. J. Chandy and P. Banerjee, "Parallel Simulated Annealing Strategies for VLSI Cell Placement", 9th Int. Conf. VLSI Design, New Delhi, India, Jan. 1996.
105. S. Ramaswamy, E. W. Hodges, and P. Banerjee, "Compiling MATLAB Programs to SCALAPACK: Exploiting Task and Data Parallelism," Proc. Int. Parallel Processing Symp. (IPPS-96), Honolulu, Hawaii, Apr. 1996, pp. 613-620.

- 106.Z. Xing and P. Banerjee, "A Parallel Hierarchical Algorithm for Module Placement Based on Sparse Linear Equations", Proc. IEEE Int. Symp. Circuits and Systems (ISCAS-96), Atlanta, GA, May 1996, Vol. IV, pp. 691-694.
- 107.V. Krishnaswamy and P. Banerjee, "Actor-based Parallel VHDL Simulation Using Time Warp," Proc. 1996 Int. Workshop on Parallel and Distributed Simulation (PADS-96), Philadelphia, PA, May, 1996.
- 108.A. Lain and P. Banerjee, "Compiler Support for Hybrid Irregular Accesses on Multicomputers" Proc. ACM Int. Conf. Supercomputing (ICS-96), Philadelphia, PA, May, 1996, pp. 1-9.
- 109.A. Roy-Chowdhury and P. Banerjee, "Compiler-Assisted Generation of Error-Detecting Parallel Programs," Proc. 26th Int. Symp. on Fault-Tolerant Computing (FTCS-26), Sendai, JAPAN, Jun. 1996.
- 110.D. Palermo, E. Su, E. W. Hodges, and P. Banerjee, "Compiler Support for Privatization for Distributed Memory Machines," Proc. Int. Conf. Parallel Processing (ICPP-96), Bloomingdale, IL, Aug. 1996.
- 111.G. Hasteer and P. Banerjee, "A Parallel Algorithm for State Assignment in Finite State Machines," Proc. Int. Conf. Parallel Processing (ICPP-96), Bloomingdale, IL, Aug. 1996.
- 112.V. Boppana, P. Saxena, P. Banerjee, W. K. Fuchs, and C. L. Liu, "A Parallel Algorithm for the Technology Mapping of LUT-based FPGAs," Proc. EUROPAR-96 Workshop on Parallel Nonnumerical Algorithms, Lyon, FRANCE, Aug. 1996.
- 113.J. A. Chandy, S. Parkes, and P. Banerjee, "Distributed Object Oriented Data Structures and Algorithms for VLSI CAD," Proc. Workshop on Parallel Algorithms for Irregularly Structured Problems, Santa Barbara, CA, Aug. 1996.
- 114.D. J. Palermo, E. W. Hodges, IV, and P. Banerjee, "Interprocedural Array Redistribution Data-Flow Analysis", Languages and Compilers for Parallel Computing, Santa Clara, CA, Aug. 1996.
- 115.P. Prabhakaran and P. Banerjee, "Parallel Algorithms for Force-Directed Scheduling of Flattened and Hierarchical Signal Flow Graphs," Proc. Int. Conf. Computer Design (ICCD-96), Austin, TX, Oct. 1996.
- 116.D. Palermo, E. W. Hodges, and P. Banerjee, "Techniques for Selecting and Analyzing Data Distributions," Workshop on Challenges in Compiling for Scalable Parallel Systems, New Orleans, LA, Oct. 1996.
- 117.K. McPherson and P. Banerjee, "Integrating Task and Data Parallelism in an Irregular Application: A Case Study", Proc. Symp. on Parallel and Distributed Processing, New Orleans, LA, Oct. 1996, pp. 208-213.
- 118.V. Krishnaswamy, R. Gupta, P. Banerjee, "A Procedure for Software Synthesis from VHDL Models," Proc. of Asia-Pacific Design Automation Conf., Tokyo, JAPAN, Jan. 1997.
- 119.G. Hasteer and P. Banerjee, "Simulated Annealing Based Parallel State Assignment for Finite State Machines," Proc. Int. Conf. VLSI Design (VLSI-97), Hyderabad, INDIA, Jan. 1997.
- 120.D. Krishnaswamy, M. S. Hsiao, V. Saxena, E. M. Rudnick, P. Banerjee, and J. Patel, "Parallel Genetic Algorithms for Simulation-based Sequential Circuit Test Generation," Proc. Int. Conf. VLSI Design (VLSI-97), Hyderabad, INDIA, Jan. 1997.
- 121.J. G. Holm, S. Parkes, and P. Banerjee, "Performance Evaluation of a C++ Library Based Multithreaded System," Hawaii Int. Conf. on System Sciences, Maui, HA, Jan. 1997.
- 122.S. Roy and P. Banerjee, "A Comparison of Parallel Approaches for Algebraic Factorization in Logic Synthesis", Proc. Int. Parallel Processing Symposium (IPPS97), Geneva, Switzerland, April 1997.

- 123.Z. Xing, J. Chandy, and P. Banerjee, "Parallel Global Routing for Standard Cells," Proc. Int. Parallel Processing Symposium (IPPS-97), Geneva, Switzerland, April 1997.
- 124.D. Krishnaswamy, E. Rudnick, P. Banerjee and J. Patel, "SPITFIRE: Scalable Parallel Algorithms for Test Set Partitioned Fault Simulation," Proc. IEEE VLSI Test Symp., Monterey, CA, Apr. 1997.
- 125.S. Roy and P. Banerjee, "An L-Shaped Partitioning-Based Algebraic Factorization Algorithm Proc. Int. Symp. on Circuits and Systems (ISCAS-97), Hong Kong, Jun. 1997.
- 126.D. Krishnaswamy, P. Banerjee, E. Rudnick and J. Patel, "Asynchronous Parallel Algorithms for Test Set Partitioned Parallel Fault Simulation," Proc. Workshop on Parallel and Distributed Simulation (PADS97), Jun. 1997.
- 127.G. Hasteer, A. Mathur, P. Banerjee, "An Efficient Assertion Checker for Combinational Properties," Proc. Design Automation Conference (DAC97), Jun. 1997.
- 128.J. G. Holm, J. Chandy, G. Hasteer, V. Krishnaswamy, S. Parkes, S. Roy, and P. Banerjee, "Performance Evaluation of Message-Driven Parallel VLSI CAD Applications on General-Purpose Multiprocessors," Proc. International Conference on Supercomputing (ICS-97), Vienna, AUSTRIA, July 1997.
- 129.D. Krishnaswamy and P. Banerjee, "Exploiting Task and Data Parallelism in Parallel Hough and Radon Transforms," Proc. Int. Conference on Parallel Processing (ICPP-97), Bloomingdale, IL, Aug. 1997.
- 130.V. Krishnaswamy, G. Hasteer, and P. Banerjee, "Load Balancing and Workload Minimization of Overlapping Parallel Tasks," Proc. Int. Conference on Parallel Processing (ICPP-97), Bloomingdale, IL, Aug. 1997.
- 131.J. A. Chandy and P. Banerjee, "A Parallel Circuit-Partitioned Algorithm for Timing-driven Standard Cell Placement," Proc. Int. Conference on Computer-Design (ICCD-97), October 1997, Austin, TX.
- 132.G. Hasteer, A. Mathur, and P. Banerjee, "A Framework for Equivalence Checking of Multi-Phase FSMs," Proc. International High-Level Design Validation and Test Workshop, Oakland, CA, Nov. 1997.
- 133.P. Prabhakaran and P. Banerjee, "Simultaneous Scheduling, Binding and Floorplanning in High-Level Synthesis," Proc. 11th International Conference on VLSI Design (VLSI Design'98), Chennai, India, Jan. 1998.
- 134.S. Roy, P. Banerjee and M. Sarrafzadeh, "Partitioning Sequential Circuits for Low Power," Proc. 11<sup>th</sup> International Conference on VLSI Design (VLSI Design'98), Chennai, India, Jan. 1998.
- 135.S. Roy, A. Harm, and P. Banerjee, "PowerShake: A Low Power Driven Clustering and Factoring Methodology for Boolean Expressions," Proc. Design, Automation and Test in Europe Conference (DATE 98), Paris, France, Feb. 1998.
- 136.D. Chakrabarti, A. Lain, and P. Banerjee, "Evaluation of Compiler and Runtime Library Approaches for Supporting Parallel Regular Applications," Proc. Int. Parallel Processing Symp. (IPPS-98), Apr. 1998, Orlando, FL, pp. 74-79.
- 137.M. Kandemir, P. Banerjee, A. Choudhary, J. Ramanujam, N. Shenoy, "A Generalized Framework for Global Communication Optimization," Proc. Int. Parallel Processing Symp. (IPPS-98), Apr. 1998, Orlando, FL, pp. 69-73.
- 138.Z. Xing and P. Banerjee, "A Parallel Algorithm for Zero Skew Clock Tree Routing," Proc. Int. Symp. Physical Design (ISPD98), Apr. 1998, Monterey, CA.
- 139.S. Roy and P. Banerjee, "Resynthesis of Sequential Circuits for Low Power," Proc. International Conference on Circuits and Systems (ISCAS-98), Monterey, CA, May 1998.

- 140.P. Prabhakaran and P. Banerjee, "Parallel Algorithms for Scheduling, Binding, and Floorplanning in High - Level Synthesis," Proc. International Conference on Circuits and Systems (ISCAS-98), Monterey, CA, May 1998.
- 141.G. Hasteer, A. Mathur, and P. Banerjee, "An Implicit Algorithm for Finding Steady States and its Application to FSM Verification," Proc. Design Automation Conference (DAC-98), Jun. 1998, San Francisco, CA.
- 142.V. Kim and P. Banerjee, "Parallel Algorithms for Power Estimation," Proc. Design Automation Conference (DAC-98), Jun. 1998, San Francisco, CA.
- 143.M. Wang, M. Sarrafzadeh, and P. Banerjee, "Placement with Incomplete Data," Proc. Design Automation Conference (DAC-98), Jun. 1998, San Francisco, CA.
- 144.V. Krishnaswamy and P. Banerjee, "Parallel Compiled Event Driven VHDL Simulation," Proc. Int. Conf. Supercomputing (ICS-98), Melbourne, AUSTRALIA, July 1998.
- 145.D. R. Chakrabarti, N. Shenoy, A. Choudhary, and P. Banerjee, "An Efficient Uniform Run-time Scheme for Mixed Regular-Irregular Applications," Proc. Int. Conf. Supercomputing (ICS-98), Melbourne, AUSTRALIA, July 1998, pp. 61-68.
- 146.M. Kandemir, A. Choudhary, N. Shenoy, J. Ramanujam, and P. Banerjee, "A Hyperplane Based Approach for Optimizing Spatial Locality in Loop Nests," Proc. Int. Conf. Supercomputing (ICS-98), Melbourne, AUSTRALIA, July 1998, pp. 69-75.
- 147.M. Kandemir, J. Ramanujam, A. Choudhary, P. Banerjee, "An iteration space transformation algorithm based on an explicit data layout representation for optimizing locality," Proc. Workshop on Languages and Compilers for Parallel Computing (LCPC-98), Chapel Hill, NC, Aug. 1998.
- 148.M. Kandemir, N. Shenoy, P. Banerjee, J. Ramanujam, and A. Choudhary, "Minimizing Data and Synchronization Costs in One-Way Communication," Proc. Int. Conf. Parallel Processing (ICPP98), Minneapolis, MN, Aug. 1998.
- 149.Z. Xing and P. Banerjee, "A Parallel Algorithm for Timing-Driven Global Routing for Standard Cells," Proc. Int. Conf. Parallel Processing (ICPP98), Minneapolis, MN, Aug. 1998, pp. 54-61.
- 150.M. Kandemir, A. Choudhary, J. Ramanujam, N. Shenoy, and P. Banerjee, "Enhancing Spatial Locality Using Data Layout Optimizations," Proc. European Conference on Parallel Processing (Euro-Par'98), Southampton, ENGLAND, Sept. 1998, pp. 180-188.
- 151.A. Mishra and P. Banerjee, "A Fault Tolerant Multi-Grid Algorithm," Proc. Parallel and Distributed Computing Systems (PDCS98), Chicago, Sep. 1998.
- 152.S. Roy, A. Harms and P. Banerjee, "A Low Power Logic Optimization Methodology Based on a Fast Power Driven Mapping," Proc. Int. Conf. Computer Design (ICCD-98), Austin, TX, Oct. 1998.
- 153.M. Kandemir, A. Choudhary, J. Ramanujam, N. Shenoy, and P. Banerjee, "A Matrix-Based Approach to the Global Locality Optimization Problem," Proc. Parallel Architectures and Compilation Techniques (PACT-98), Paris, FRANCE, Oct. 1998.
- 154.S. Roy and P. Banerjee, "Power Drive: A fast, canonical POWER estimator for DRIVING synthEsis," Proc. 1998 International Conference on Computer-Aided Design (ICCAD-98), San Jose, CA, Nov. 1998.
- 155.G. Hasteer, A. Mathur, and P. Banerjee, "Efficient Equivalence Checking of Multi-Phase Designs Using Retiming", Proc. 1998 International Conference on Computer-Aided Design (ICCAD-98), San Jose, CA, Nov. 1998.

- 156.D. Chakrabarti, P. Joisha, J. Chandy, D. Krishnaswamy, V. Krishnaswamy, and P. Banerjee, "WADE: A Web-Based Automated Parallel CAD Environment," Proc. International Conference on High Performance Computing (HiPC'98), Chennai, INDIA, Dec. 1998.
- 157.M. Kandemir, A. Choudhary, J. Ramanujam, and P. Banerjee, "Improving Locality Using Loop and Data Transformations in an Integrated Framework" Proc. 31st International Symposium on Micro-Architecture (MICRO-31), Dallas, Texas, Dec. 1998.
- 158.P. Prabhakaran, J. Crenshaw, P. Banerjee, and M. Sarrafzadeh, "Simultaneous Scheduling, Binding and Floorplanning for Interconnect Power Optimization," Proc. 1999 VLSI Design Conference, Goa, INDIA, Jan. 1999.
- 159.Y. Yuan and P. Banerjee, "ICE: Incremental 3-Dimensional Capacitance and Resistance Extraction for an Iterative Design Environment," Proc. 9th Great Lakes Symposium on VLSI, Ann Arbor, MI, March 1999.
- 160.J. Crenshaw, M. Sarrafzadeh, P. Banerjee, and P. Prabhakaran, "An Incremental Floor-Planner," Proc. 9th Great Lakes Symposium on VLSI, Ann Arbor, MI, March 1999.
- 161.Y. Yuan and P. Banerjee, "Fast Potential Integrals for Signal Integrity Analysis," Proc. ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU'99), Monterey, CA, March 1999.
- 162.D. Chakrabarti and P. Banerjee, "A Novel Compilation Framework for Supporting Semi-Regular Distributions in Hybrid Applications," Proc. 1999 International Parallel Processing Symposium (IPPS'99), San Juan, Puerto Rico, April 1999, pp. 597-602.
- 163.M. Kandemir, A. Choudhary, J. Ramanujam, and P. Banerjee, "A Graph Based Framework to Detect Optimal Memory Layouts for Improving Data Locality," Proc. 1999 International Parallel Processing Symposium (IPPS'99), San Juan, Puerto Rico, April 1999, pp. 738-743.
- 164.P. Joisha and P. Banerjee, "PARADIGM (version 2.0): A New HPF Compilation System," Proc. 1999 International Parallel Processing Symposium (IPPS'99), San Juan, Puerto Rico, April 1999, pp. 609-615.
- 165.Y. Yuan and P. Banerjee, "Incremental Capacitance Extraction and Its Application to Iterative Timing Driven Detailed Routing," 1999 International Symposium on Physical Design (ISPD-99), Monterey, CA, April 1999.
- 166.J. Chen and P. Banerjee, "Parallel Construction Algorithms for BDDs," 1999 International Symposium on Circuits and Systems (ISCAS'99), Orlando, FL, June 1999.
- 167.S. Roy, A. Harms, and P. Banerjee, "An ff-approximate Algorithm for Delay-Constraint Technology Mapping," Proc. 1999 Design Automation Conference (DAC'99), Jun. 1999.
- 168.A. Mishra and P. Banerjee, "An Algorithm Based Error Detection Scheme for the Multigrid Method," Proc. of the 1999 International Symposium on Fault Tolerant Computing, Madison, WI, June 15-18, 1999.
- 169.M. Kandemir, P. Banerjee, A. Choudhary, J. Ramanujam, and E. Ayguade, "An ILP Approach for Optimizing Cache Locality," 1999 ACM International Conference on Supercomputing (ICS'99), Rhodes, Greece, June 1999.
- 170.D. Chakrabarti and P. Banerjee, "Accurate Data and Context Management in Message Passing Programs," Proc. Languages and Compilers for Parallel Computing (LCPC-99), La Jolla, CA, Aug. 1999.
- 171.M. Kandemir, A. Choudhary, J. Ramanujam, and P. Banerjee, "A Framework for Interprocedural Locality Optimization Using Both Loop and Data Layout Transformations," Proc. 1999 International Conference on Parallel Processing (ICPP'99), Aizu, JAPAN, Sept. 1999, pp. 95-102.

- 172.M. Kandemir, A. Choudhary, J. Ramanujam, and P. Banerjee, "On Reducing False Sharing While Improving Locality on Shared Memory Multiprocessors," Proc. 1999 International Conference on Parallel Architectures and Compilation Techniques (PACT'99), Newport Beach, CA, Oct. 12-16, 1999.
- 173.S. Periyayacheri, A. Nayak, A. Jones, N. Shenoy, A. Choudhary, and P. Banerjee, "Library Functions in Reconfigurable Hardware for Matrix and Signal Processing Operations in MATLAB," 11th IASTED Parallel and Distributed Computing and Systems Conference (PDCS'99), Cambridge, MA, Nov. 1999.
- 174.Y. Yuan and P. Banerjee, "A Parallel 3-D Capacitance Extraction Program," Proc. 6th International Conference on High Performance Computing (HiPC'99), Calcutta, INDIA, Dec. 1999.
- 175.Z. Ye, N. Shenoy, and P. Banerjee, "A C Compiler for a Processor with a Reconfigurable Functional Unit," Proc. ACM/SIGDA Symposium on Field Programmable Gate Arrays, Monterey, CA, Feb. 2000.
- 176.N. Shenoy, A. Choudhary, and P. Banerjee, "A System-Level Synthesis Algorithm with Guaranteed Solution Quality," Proc. Design Automation and Test in Europe (DATE 2000), Paris, FRANCE, March 27-30, 2000.
- 177.M. Haldar, A. Nayak, A. Choudhary, and P. Banerjee, "Parallel Algorithms for FPGA Placement," Proc. Great Lakes Symposium on VLSI (GVLSI 2000), Chicago, IL, March 2000.
- 178.P. Banerjee, N. Shenoy, A. Choudhary, S. Hauck, M. Haldar, P. Joisha, A. Jones, A. Kanhere, A. Nayak, S. Periyacheri, M. Walkden, and D. Zaretsky, "A MATLAB Compiler for Distributed Heterogeneous Reconfigurable Computing Systems," Int. Symp. on FPGA Custom Computing Machines (FCCM-2000), Napa Valley, CA, Apr. 2000.
- 179.Y. Yuan and P. Banerjee, "A Parallel Implementation of A Fast Multipole Based 3-D Capacitance Extraction Program on Distributed Memory Multicomputers," Proc. 14th International Parallel and Distributed Processing Symposium (IPDPS 2000), Cancun, MEXICO, May 1-5, 2000 (Best Paper Award).
- 180.Z. Ye, P. Banerjee, S. Hauck, and A. Moshovos, "CHIMAERA: A High-Performance Architecture with a Tightly-Coupled Reconfigurable Functional Unit," Proc. 27th International Symposium on Computer Architecture, Vancouver, CANADA, June 10-14, 2000.
- 181.P. Joisha, A. Kanhere, P. Banerjee, N. Shenoy, and A. Choudhary, "Handling Context-Sensitive Syntactic Issues in the Design of a Front-end for a MATLAB Compiler," Proc. ACM Array Programming Languages Conference (APL-Berlin-2000), Berlin, GERMANY, July 24-27, 2000.
- 182.A. Nayak, M. Haldar, A. Kanhere, P. Joisha, N. Shenoy, A. Choudhary, and P. Banerjee, "A Library Based Compiler to Execute MATLAB Programs on a Heterogeneous Platform," Proc. ISCA 13th International Conference on Parallel and Distributed Computing Systems (PDCS-2000), Las Vegas, NE, Aug. 8-10, 2000.
- 183.A. Nayak, P. Banerjee, C. Chen, and M. Sarrafzadeh, "Power Optimization Issues in Dual Voltage Design," International Conference on Design Automation (ICDA 2000), Beijing, CHINA, Aug. 21-25, 2000.
- 184.M. Haldar, A. Nayak, A. Kanhere, P. Joisha, N. Shenoy, A. Choudhary, and P. Banerjee, "MATCH Virtual Machine: An Adaptive Runtime System to Execute MATLAB in Parallel," Proc. International Conference on Parallel Processing (ICPP-2000), Toronto, CANADA, Aug. 2000.
- 185.V. Kim, P. Banerjee, and K. De, "Fine-Grained Parallel VLSI Synthesis for Commercial CAD on a Network of Workstations," Proc. International Conference on Parallel Processing (ICPP-2000), Toronto, CANADA, Aug. 2000.
- 186.P. Joisha, and P. Banerjee, "Efficient Computation of Ownership Sets in HPF," Proc. Languages and Compilers for Parallel Computing (LCPC-2000), Aug. 2000, Yorktown Heights, New York.

187. Y. Yuan and P. Banerjee, "Comparative Study of Parallel Algorithms for 3-D Capacitance Extraction on Distributed Memory Multiprocessors," Proc. International Conference on Computer Design (ICCD'2000), Austin, TX, Sept. 17-20, 2000.
188. A. Nayak, M. Haldar, P. Banerjee, C. Chen, and M. Sarrafzadeh, "Power Optimization of Delay Constrained Circuits," Proc. Application Specific Integrated Circuit/System-on-a-Chip Conference (ASCI/SOC 2000), Washington, DC, September 2000.
189. V. Kim, P. Banerjee, K. De, and J. Brouwers, "Parallel and Distributed VLSI Synthesis for Commercial CAD on a Network of Workstations," Proc. 12th IASTED International Conference on Parallel and Distributed Computing Systems (PDCS 2000), Las Vegas, NV, November 6-9, 2000.
190. M. Haldar, A. Nayak, A. Choudhary, and P. Banerjee, "Scheduling Algorithms for Automated Synthesis of Pipelined Designs on FPGAs for Applications Described in MATLAB", Proc. International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES 2000), Nov. 2000, San Jose, CA.
191. M. Haldar, A. Nayak, N. Shenoy, A. Choudhary, and P. Banerjee, "FPGA Hardware Synthesis from MATLAB," Proc. of VLSI Design Conf. Jan. 2001, Bangalore, India.
192. N. Shenoy, P. Banerjee, A. Choudhary, and M. Kandemir, "Efficient Synthesis of Array Intensive Computations onto FPGA Based Accelerators," Proc. of VLSI Design Conf. Jan. 2001, Bangalore, India.
193. M. Haldar, A. Nayak, A. Choudhary, and P. Banerjee, "Automated Synthesis of Pipelined Designs on FPGAs for Signal and Image Processing Applications Described in MATLAB," Proc. Asia Pacific Design Automation Conf (ASP-DAC), Feb. 2001, Tokyo, Japan.
194. M. Haldar, A. Nayak, A. Choudhary, and P. Banerjee, "FPGA Hardware Synthesis from MATLAB Utilizing Optimized IP Cores" Proc. Ninth ACM/SIGDA International Symposium on Field Programmable Gate Arrays., Feb. 2001, San Jose, CA.
195. A. Nayak, M. Haldar, A. Choudhary, P. Banerjee, "Precision And Error Analysis Of MATLAB Applications During Automated Hardware Synthesis for FPGAs," Proc. Design Automation and Test in Europe (DATE 2001), Mar. 2001, Berlin, Germany.
196. A. Nayak, M. Haldar, A. Choudhary and P. Banerjee, "Parallelization of MATLAB Applications for a Multi-FPGA System," Proc. FPGA Symp. on Custom Computing Machines (FCCM-2001), Napa Valley, CA, Apr. 2001.
197. P. Joisha and P. Banerjee, "Correctly Detecting Intrinsic Type Errors in Typeless Languages Such as MATLAB," Proc. of the APL Conference, New Haven, CT, Jun. 2001.
198. D. Chakrabarti and P. Banerjee, "Global Optimization Techniques for Automatic Parallelization of Hybrid Applications," Proc. Int. Conf. Supercomputing, Jun. 2001, Sorrento, Italy.
199. P. G. Joisha, P. Banerjee, "Computing Array Shapes in MATLAB", Proc. of the Int. Workshop on Languages and Compilers for Parallel Computing (LCPC), Cumberland Falls, USA. August 2001. In Springer-Verlag Lecture Notes in Computer Science Series.
200. A. K. Jones, and P. Banerjee, "Parallel Implementation of Matrix and Signal Processing Libraries on FPGAs," Proc. IASTED Parallel and Distributed Computing Systems Conf. (PDCS2001), Anaheim, CA, Aug. 2001.
201. P. Banerjee, M. Haldar, A. Nayak, A. Choudhary, "Overview of the MATCH Compiler for Compiling MATLAB Programs into Hardware," Proc. of NASA Earth Science Technology Conference, Aug. 2001, Washington, DC.

- 202.M. Haldar, A. Nayak, A. Choudhary, P. Banerjee, "A System for Synthesizing Optimized FPGA Hardware from MATLAB," Proc. Int. Conf. on Computer Aided Design, Nov. 4-8, 2001, San Jose, CA.
- 203.A. Nayak, M. Haldar, A. Choudhary, and P. Banerjee, "Accurate Area and Delay Estimators for FPGAs," Proc. Design Automation and Test in Europe (DATE-2002), Mar. 2002, Paris, France.
- 204.A. Jones, D. Bagchi, S. Pal, X. Tang, A. Choudhary, and P. Banerjee, "PACT HDL: A C Compiler with Power and Performance Optimizations," Proc. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2002), Grenoble, France, October 2002.
- 205.P. Banerjee, M. Haldar, A. Nayak, V. Kim, D. Bagchi, S. Pal, N. Tripathi, "A Behavioral Synthesis Tool For Exploiting Fine Grain Parallelism in FPGAs," Proc. International Workshop on Distributed Computing (IWDC), Dec. 28-30, 2002, Kolkata, INDIA. To Appear as Springer Verlag Lectures in Computer Science Series.
- 206.P. Banerjee, "An Overview of a Compiler for Mapping MATLAB Programs onto FPGAs," Invited Paper at the Asia Pacific Design Automation Conference (ASP-DAC03), Jan. 2003, Japan.
207. P. Banerjee, M. Haldar, A. Nayak, V. Kim, J. Uribe, "AccelFPGA: A DSP Design Tool for Making Area Delay Tradeoffs While Mapping MATLAB Programs onto FPGAs," Proc. International Signal Processing Conference (ISPC) and Global Signal Processing Expo (GSPx), Mar. 31-Apr. 3, 2003, Dallas, TX.
- 208.P. Banerjee, V. Saxena, J. Uribe, M. Haldar, A. Nayak, V. Kim, D. Bagchi, S. Pal, N. Tripathi, R. Anderson, "Making Area-Performance Tradeoffs at the High Level Using the AccelFPGA Compiler for FPGAs," Proc. 11th ACM International Symposium on Field Programmable Gate Arrays (FPGA 03), Poster Paper. Monterey, CA, Feb. 2003.
- 209.P. G. Joisha, and P. Banerjee, "The MAGICA Type Inference Engine for MATLAB," Proc. International Conference on Compiler Construction (CC 03), Warsaw, Poland, Apr. 2003.
- 210.P. Banerjee, D. Bagchi, M. Haldar, A. Nayak, V. Kim, R. Uribe, "Automatic Conversion of Floating Point MATLAB Programs into Fixed Point FPGA Based Hardware Design," Proc. FPGA based Custom Computing Machines (FCCM), Apr. 2003, Monterey, CA.
211. A. K. Jones, P. Banerjee. An Automated and Power-Aware Framework for Utilization of IP Cores in Hardware Generated from C Descriptions Targeting FPGAs, Proc. FPGA based Custom Computing Machines (FCCM), Apr. 2003, Monterey, CA.
212. P. G. Joisha, P. Banerjee, "Static Array Storage Optimization in MATLAB," Proc. ACM SIGPLAN 2003 Conference on Programming Language Design and Implementation (PLDI 03), San Diego, CA, June 2003.
213. X. Tang, T. Jiang, A. K. Jones, P. Banerjee, "Compiler Optimizations in the PACT HDL Behavioral Synthesis Tool for ASICs and FPGAs," Proc. IEEE System on a Chip Conference, Portland, OR., Sep. 2003.
- 214.T. Jiang, X. Tang, A. K. Jones, P. Banerjee, "Optimizing Power While Exploiting Fine Grain Parallelism in FPGAs" Proc. Int. Conf. Parallel and Distributed Computing Systems (PDCS), Marina Del Rey, CA, Nov. 2003.
- 215.R. Mukherjee, A. K. Jones, P. Banerjee, "System Level Synthesis of Multiple IP Blocks in the PACT Compiler," Proc. Int. Conf. Parallel and Distributed Computing Systems (PDCS03), Marina Del Rey, CA, Nov. 2003
- 216.N. Liveris, P. Banerjee, "Power Aware Interface Synthesis for Bus Based SOC Design," Proc. Design Automation and Test in Europe (DATE 2004), Feb. 2004, Paris, FRANCE.

217. T. Jiang, X. Tang, P. Banerjee, "High Level Area, Delay and Power Estimation for FPGAs," Proc. Int. Conf. on Field Programmable Gate Arrays (FPGA-2004), Monterey, CA, Feb. 2004.
218. S. Roy, D. Sinha and P. Banerjee, "An Algorithm for Trading off Quantization Error in MATLAB based Hardware Design," Proc. Int. Conf. on Field Programmable Gate Arrays (FPGA-2004), Monterey, CA, Feb. 2004.
219. R. Mukherjee, A. K. Jones, P. Banerjee, "Handling Data Streams While Compiling C Programs Onto Hardware" Proc. IEEE Int. Symp. on VLSI (ISVLSI), Feb. 19-20, 2004; Lafayette, LA, USA
220. A. K. Jones, X. Tang, P. Banerjee, "Compile-time Simulation for Low-Power Optimization using SystemC," Proc. IASTED International Conference on Modeling and Simulation (MS 2004), March 2004, Marina del Rey, CA.
221. T. Jiang, X. Tang, P. Banerjee, "High Level Area and Power Estimation for FPGAs," Proc. Great Lakes Symp. on VLSI (GLSVLSI 2004), April 26-28, 2004, Boston, MA, USA.
222. D. Zaretsky, G. Mittal, X. Tang, P. Banerjee, "Evaluation of Scheduling and Allocation Algorithms While Mapping Software Assembly onto FPGAs," Proc. Great Lakes Symp. on VLSI (GLSVLSI 2004), April 26-28, 2004, Boston, MA, USA.
223. D. Zaretsky, G. Mittal, X. Tang, and P. Banerjee, "Overview of the FREEDOM Compiler for Mapping DSP software to FPGAs," Proc. IEEE Conference on FPGA based Custom Computing Machines (FCCM), Napa Valley, Apr. 2004.
224. G. Mittal, D. Zaretsky, X. Tang, and P. Banerjee, "Automatic Translation of Software Binaries onto FPGAs," Proc. Design Automation Conference (DAC 2004), San Diego, Jun. 2004.
225. S. Roy and P. Banerjee, "An Algorithm for Converting Floating Point Computations to Fixed Point Computations in MATLAB based Hardware Design," Proc. Design Automation Conference (DAC 2004), San Diego, Jun. 2004.
226. P. Banerjee, G. Mittal, D. Zaretsky, X. Tang, "BINACHIP-FPGA: A Tool to Map DSP Software Binaries and Assembly Programs onto FPGAs," Proc. Embedded Signal Processing Conference (GSPx), Sep. 2004, Santa Clara, CA.
227. X. Tang, T. Jiang, A. K. Jones, P. Banerjee, "Behavioral Synthesis of Data-Dominated Circuits for Minimal Energy Implementation," Proc. 18<sup>th</sup> International Conference on VLSI Design (VLSI 2005), Jan. 2005, Kolkata, India.
228. G. Mittal, D. Zaretsky, P. Banerjee, "Automatic Extraction of Function Bodies from Software Binaries," Proc. Asia Pacific Design Automation Conference (ASP-DAC 2005), Jan. 2005, Shanghai, China.
229. X. Tang, H. Zhou, and P. Banerjee, "Leakage Power Optimization with Dual Vth Library during High Level Synthesis," Proc. IEEE/ACM Design Automation Conf, Jun. 2005, Anaheim, CA.
230. D. Zaretsky, G. Mittal, R. P. Dick and P. Banerjee, "Generation of Control and Data Flow Graphs from Scheduled Pipelined Assembly Code," Proc. 18<sup>th</sup> Int. Workshop on Languages and Compilers for Parallel Computing (LCPC 2005), Oct. 2005, Hawthorne, NY.
231. G. Mittal, D. Zaretsky, and P. Banerjee, "Tool-flow For an Automated Compilation of SIMULINK and Real-Time Workshop Applications onto Heterogeneous Platforms," Proc. GSPx 2005 Pervasive Signal Processing Conference, Oct. 2005, Santa Clara, California,
232. N. Liveris, H. Zhou, P. Banerjee, "An Efficient System-level to RTL Verification Framework for Computation-Intensive Applications," Proc. Asian Test Symposium, Dec. 18-21, 2005 in Kolkata, India.

233. D. Zaretsky, G. Mittal, R. P. Dick and P. Banerjee, "Dynamic Template Generation for Resource Sharing in Control and Data Flow Graphs," Proc. Int. Symp. On VLSI Design (VLSI 2006), Jan. 2006, Hyderabad, INDIA.

234. A. Mallik, D. Sinha, H. Zhou, and P. Banerjee, "Smart Bit-width Allocation for Low Power Optimization in a SystemC based ASIC design Environment", Proc. Design Automation and Test in Europe (DATE), Mar. 2006, Munich, Germany.

#### **PATENT APPLICATIONS**

1. P. Joisha, P. Banerjee, N. Shenoy, "Method for Array Shape Inferencing for a Class of Functions in MATLAB." Reference Number NWU-P005, Patent Filed: January 31, 2001 (No decisions)

## SUMMARY OF INFORMATION

Prith Banerjee received his B.Tech. degree in Electronics and Electrical Engineering from the Indian Institute of Technology, Kharagpur, India, in August 1981, and the M.S. and Ph.D degrees in Electrical Engineering from the University of Illinois at Urbana-Champaign in December 1982 and December 1984 respectively.

Prith Banerjee is currently Dean of the College of Engineering at the University of Illinois at Chicago (UIC), and UIC Distinguished Professor. In this role, he leads the UIC College of Engineering which consists of about 115 faculty in six engineering department and 6 research centers, 1,550 undergraduate and 900 graduate students.

Previously, Dr. Banerjee was the Walter P. Murphy Professor and chairman of electrical and computer engineering at Northwestern University, where he was also director of the Center for Parallel and Distributed Computing. Prior to that, he was the Director of the Computational Science and Engineering program, and Professor of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign

In 2000, Prith founded AccelChip, Inc., ([www.accelchip.com](http://www.accelchip.com)) a developer of products and services for electronic design automation. He served as president and CEO of AccelChip while on leave from Northwestern from 2000 to 2002, during which time he raised \$2.3 million of financing, helped the company build its first product and saw the company grow to 25 employees and \$800,000 in revenues. He remained as a consultant to AccelChip in the role of chief scientist. Accelchip was acquired by Xilinx Corporation in Jan. 2006 for \$21.5 million. In addition, he has been on the Technical Advisory Boards of many companies such as Atrenta, Calypto Design Systems, and Ambit Design Systems. In 2004, he started another company, BINACHIP, where he is serving in the role of Founder, Chairman and Chief Scientist.

Dr. Banerjee's research interests are in Parallel Algorithms for VLSI Design Automation, Distributed Memory Parallel Compilers, and Compilers for Adaptive Computing, and is the author of over 300 papers in these areas. He leads the PARADIGM compiler project for compiling programs for distributed memory multicomputers, the ProperCAD project for portable parallel VLSI CAD applications, the MATCH project on a MATLAB compilation environment for adaptive computing, the PACT project on power aware compilation of hardware and software, and the FREEDOM compiler project on compiling software binaries to hardware.. He is also the author of a book entitled "Parallel Algorithms for VLSI CAD" published by Prentice Hall, Inc., 1994.

Dr. Banerjee has received numerous awards and honors during his career. He became a Fellow of the AAAS in 2006, and a Fellow of the ACM in 2000. He was the recipient of the 1996 Frederick Emmons Terman Award of ASEE's Electrical Engineering Division sponsored by Hewlett-Packard. He was elected to the Fellow grade of IEEE in 1995. He received the University Scholar award from the University of Illinois for in 1993, the Senior Xerox Research Award in 1992, the IEEE Senior Membership in 1990, the National Science Foundation's Presidential Young Investigators' Award in 1987, the IBM Young Faculty Development Award in 1986, and the President of India Gold Medal from the Indian Institute of Technology, Kharagpur, in 1981.

Dr. Banerjee has served as the Program Chair of the High-Performance Computing Conference in 1999, and Program Chair of the Int. Conf. on Parallel Processing for 1995. He has served as General Chairman of the International Conference on Parallel and Distributed Computing Systems in 1997, and the International Workshop on Hardware Fault Tolerance in Multiprocessors, 1989. He has served on the Program and Organizing Committees of the 1988, 1989, 1993 and 1996 Fault Tolerant Computing Symposia, the 1992, 1994, 1995, 1996 and 1997 International Parallel Processing Symposium, the 1991, 1992, 1994 and 1998 International Symposia on Computer Architecture, the 1998 International Conference on Architectural Support of Programming Languages and Operating Systems, the 1990, 1993, 1994, 1995, 1996, 1997 and 1998 International Symposium on VLSI Design, the 1994, 1995, 1996, 1997, 1998 and 2000 International Conference on Parallel Processing, and the 1995, 1996 and 1997 International Conference on High-Performance Computing. He is an Associate Editor of the IEEE Transactions on Parallel and Distributed Systems, and IEEE Transactions on Computers. In the past he has served as Associate Editor of the Journal of Parallel and Distributed Computing, the IEEE Transactions on VLSI Systems, and the Journal of Circuits, Systems and Computers.

Prith has served on the Technical Advisory Board of many companies such as Ambit Design Systems, Calypto Design Systems, and Atrenta.

Prith has received research grants worth about \$4.0 million during his 12 years at Illinois with him as a principal investigator. He has received about \$8.0 million at Northwestern University during the past 4 years. His funding has come from national agencies such as DARPA, NSF, ONR, NASA and industries such as IBM, Intel, General Electric, and SRC.

He has completed the supervision of 35 Ph.D. and 40 M.S. students.

## SUMMARY OF RESEARCH

Professor Prith Banerjee has performed research on Parallel Algorithms, Parallel Compilers, and Parallel Architectures, and Compilers for Adaptive Computing. He has published over 300 papers in premier journals and conferences. In the following, his main research accomplishments are summarized.

**(1) Parallel Algorithms for VLSI CAD.** As VLSI circuits become more complex, the computational requirements for performing various CAD tasks increase almost exponentially. Professor Banerjee has investigated efficient parallel algorithms for various tasks in VLSI computer-aided design in order to reduce the runtimes of these tools for future billion transistor VLSI chips from weeks to hours. He has written a graduate level textbook on the subject, "Parallel Algorithms for VLSI CAD," published by Prentice Hall, 1994. As part of the PROPERCAD project, he has developed portable parallel algorithms that are suitable for execution on distributed memory message-passing multicomputers, networks of workstations, and shared-memory multiprocessors. His most significant publications in this area include his work on parallel simulated annealing algorithms for standard cell placement where he proposed and evaluated several parallel strategies such as parallel moves, speculative computation and multiple markov chains approaches. In his work on parallel algorithms for test generation of combinational and sequential circuits, he proposed how a parallel branch and bound algorithm for test generation can be efficiently integrated within a parallel fault simulation environment. He has worked on parallel circuit extraction and design rule checking, where he developed strategies for exploiting data parallelism on flattened layouts, and task parallelism on hierarchical layouts, and sophisticated scheduling for combining task and data parallelism. He has also worked on parallel algorithms for global and detailed routing using iterative improvement, parallel algorithms for combinational and sequential logic synthesis using the MIS and transduction algorithms, parallel algorithms for behavioral simulation using VHDL, and on parallel algorithms for high-level synthesis. Dr. Banerjee published more than 100 papers in this area; two of these papers have received the Best Paper Awards at conferences, one for his work on "SPITFIRE: Scalable Parallel Algorithms for Test Set Partitioned Fault Simulation" at the IEEE VLSI Test Symposium in 1997, and another for his work on "A Parallel Implementation of A Fast Multipole Based 3-D Capacitance Extraction Program on Distributed Memory Multicomputers" at the IEEE Int. Parallel and Distributed Symposium in 2000. Prith's work in this area was supported by DARPA, NSF, and the Semiconductor Research Corporation. He has worked closely with many companies including the Cadence, LSI Logic, Ambit Design Systems, and Sunrise Test Systems, to develop these parallel algorithms and have transferred many of these algorithms to industry. For example, LSI Logic has a commercial product called Parallel Gate-Ensemble which is based on the parallel cell placement algorithms developed by him. Cadence Design Systems has a product called parallel VAMPIRE which is based on some of the parallel design rule checking algorithms developed by him. Finally, he has worked with Ambit Design Systems to develop a product called Distributed Buildgates for parallel logic synthesis. The Design Sciences Program of the Semiconductor Research Corporation listed the ProperCAD project under Professor Banerjee as one of the two key Technical Innovations during the 1994 year, and was included in the SRC Corporate Annual Report. More information about the ProperCAD project can be found at: <http://www.ece.nwu.edu/cpdc/ProperCAD/pcad.html>.

**(2) Parallelizing Compilers.** Distributed memory message passing machines such as the Intel Paragon, and the IBM SP-2 and networks of workstations offer significant advantages over shared-memory multiprocessors in terms of cost and scalability. Unfortunately, to extract all that computational power from these machines, users have to write efficient software for them, which is an extremely laborious process. As part of the PARADIGM compiler project, Prof. Banerjee has developed strategies by which sequential programs written in Fortran 77 or High Performance Fortran can be automatically parallelized and compiled for efficient execution on distributed memory message-passing multicomputers and networks of workstations. His most significant publications in this area include his work on automated data distribution on distributed memory multi-processors, where he developed a constraint-based approach for deriving the static and dynamic distributions of regular data structures using simple computation and communication cost models. He has also developed strategies where the PARADIGM compiler can automatically

extract data and functional parallelism simultaneously from Fortran programs using a convex programming formulation. His other significant contribution is in the development of an uniform framework for supporting both regular and irregular data accesses using an interval based runtime library using the inspector-executor approach. He has recently developed strategies for unified loop and data transformations for improving cache locality in distributed shared memory multiprocessors. Prith's work on the PARADIGM compiler is one of five leading research projects in academia in this area of parallelizing compilers for distributed memory multiprocessors; this includes Ken Kennedy's work on the Fortran D compiler at Rice, Monica Lam's work on SUIF at Stanford, Joel Saltz's work on CHAOS/PARTI at Maryland, David Padua's work on the Polaris compiler at Illinois, and Hans Zima's work on the Vienna Fortran compiler in Europe. Prith's work has been supported by DARPA, NSF and various companies. He has published more than 80 papers in this area (out of 270 total papers in his career), one of which received a Best Paper Award at the International Conference on Parallel Processing in 1994 for the paper entitled "Communication Optimizations for Distributed Memory Multicomputers in the PARADIGM Compiler." He has worked closely with many companies including IBM, Kuck and Associates, and Portland Group, to develop various compiler techniques, and has transferred many of these techniques to industry. Specifically, the automatic data partitioning and static cost estimation work was transferred to IBM T.J. Watson Center (by Manish Gupta) in the IBM xlf HPF compiler. The PARADIGM compiler has been licensed to a company, Tata Information Systems Ltd., for commercial development. More information about the PARADIGM project can be found at: <http://www.ece.nwu.edu/cpdc/Paradigm/Paradigm.html>

**(3) MATLAB Compiler for Reconfigurable Computing.** Digital signal processing and image processing applications are typically written in the MATLAB programming language, and are typically executed on general purpose DSP processors. However, recently DSP algorithms are being mapped onto Reconfigurable Field Programmable Gate Arrays (FPGAs) for performance and reconfigurability reasons. However, to map DSP algorithms onto FPGAs, users are required to manually translate MATLAB programs onto languages such as VHDL or Verilog. As part of the MATCH project, Professor Banerjee has the MATCH compiler that takes MATLAB programs and automatically parallelizes it and maps it a heterogeneous environment of off-the-shelf embedded processors, digital signal processors, and FPGAs. More details of the MATCH project can be found at the URL: <http://www.ece.northwestern.edu/cpdc/Match/Match.html>. He has transferred this technology to a new company he has founded called Accelchip ([www.accelchip.com](http://www.accelchip.com)) which has developed a successful product called AccelFPGA based on the MATCH compiler.

**(4) Compiler for Power Aware Computing.** Low power electronic circuits are becoming very desirable in the domain of mobile wireless devices. Current electronic design tools have two limitations: (1) They require the designers to enter their designs at the register transfer level in languages such as VHDL or Verilog (2) They perform area minimizations under timing constraints or perform timing optimizations under area constraints. As part of the PACT compiler project, Prith Banerjee is developing a compiler that will take a high-level language, namely, C, and automatically produce Register Transfer Level VHDL and Verilog code that can be mapped onto FPGAs and ASICs. Furthermore, this transformation will be performed under power, area and timing constraints. More details of the MATCH project can be found at the URL: <http://www.ece.northwestern.edu/cpdc/PACT/PACT.html>

**(5) Compiling Software Binaries onto Hardware.** Increasing demands for cell-phones, PDAs, and network devices have provided opportunities for the growth of embedded software, operating systems and development tools. As newer processor architectures are announced, there is a need to reuse and migrate the software from older generation processors to newer processors. In this research we will develop automated compiler algorithms to translate software binary and assembly code of a general-purpose processor into Register Transfer Level VHDL and Verilog code to be mapped onto hardware in the form of FPGAs and ASICs. We further plan to study techniques for performing hardware/software co-design and verification on integrated Systems-on-a-Chip (SOC) platforms consisting of embedded processors, memories, FPGAs and ASICs. We are demonstrating our concepts using a prototype FREEDOM compiler that will translate binary code of a Texas Instruments TMS320 C6000 processor into a hardware/software implementation on a Xilinx Virtex II Pro SOC. More details of the FREEDOM project can be found at the URL: <http://www.ece.northwestern.edu/cpdc/FREEDOM/FREEDOM.html>

## CONTRIBUTIONS AS AN ADMINISTRATOR

Prith Banerjee has had wide ranging experience as an administrator. He has served as

- Director the Computational Science and Engineering Program at the University of Illinois from 1994 to 1996.
- Director of the Center for Parallel and Distributed Computing at Northwestern University from 1996-present
- Chairman of the Electrical and Computer Engineering department at Northwestern University from 1998-2001 and 2002-present
- President and CEO of AccelChip from 2000 to 2002.
- Dean, College of Engineering, University of Illinois at Chicago, from 2004-present.

In the following his contributions as an administrator will be described in more detail.

Prith Banerjee was instrumental in the development of a new graduate program at the University of Illinois called Computational Science and Engineering. The term Computational Science and Engineering (CSE) refers to those activities in science and engineering that exploit computing as their main tool. The purpose of the graduate option in CSE at the University of Illinois was to develop an academic program that prepares students with an interdisciplinary background in numerical computing, high performance software and parallel computing, and computational aspects of various applications. Prof. Banerjee was the founding Director of the CSE program at Illinois during 1994-96. During those two years, he was successful in establishing the CSE academic program in ten departments, creating/identifying more than 40 CSE courses, sponsoring 8 research assistantships for CSE research activities, writing research proposals to obtain advanced computing equipment for a CSE laboratory, starting a CSE seminar, and writing proposals to acquire grants for research in CSE. Through his efforts, he was able to procure the donation of 10 workstations from IBM, and a 24 processor Paragon multiprocessor from Intel, a SUN Sparcserver 8 processor multiprocessor, and a dozen SUN workstations.

During Sep. 1, 1996 to Aug. 15, 2004, Prof. Banerjee was the Director of the Center for Parallel and Distributed Computing at Northwestern University. The Center has 11 faculty from Northwestern and two scientists from Argonne National Lab. The Center has attracted three large DARPA grants worth about \$2 million each, namely the MATCH compiler project, the CHIMAERA project, and the PACT compiler project. In addition, he has brought in a \$1 million NSF grant on the PANTHER project, and a \$1 million DOE grant to support research on a wide range of topics in high-performance computing.

During Sep. 1, 1998 to Aug. 31, 2001, and from September 1, 2002 to August 15, 2004, Prof. Banerjee was the Chairman of the Electrical and Computer Engineering Department at Northwestern University. During these five years, he has led the development of some innovative revisions of the electrical engineering and computer engineering undergraduate curricula at Northwestern. He has been responsible for leading the creation of two freshman courses ECE 202 on "Introduction to Electrical Engineering" and ECE 203 on "Introduction to Computer Engineering". The ECE 202 course teaches electrical engineering to freshman students using the design of a CD player, and the ECE 203 course teaches computer engineering to freshmen using the design of an autonomous robot. During 1998-99, he personally attended weekly meetings of two committees, the undergraduate electrical engineering committee, and the undergraduate computer engineering committee, which designed the new curriculum and the courses. He has also been instrumental in making major renovations in the instructional labs of the department by securing equipment donations from companies such as Hewlett-Packard, Motorola and Microsoft, and obtaining significant funding from the President of Northwestern University. In addition, he was instrumental in hiring 11 new faculty in the department (including 2 women), 6 of whom have won the NSF CAREER awards. During this period the rankings of the ECE Department have gone up to 17<sup>th</sup> in Computer Engineering and 20<sup>th</sup> in Electrical Engineering according to US News and World Reports.

Since August 16, 2004, Prith Banerjee has been Dean of the College of Engineering. In this role, he is responsible for six academic departments and 8 research centers, 115 faculty, 1550 undergraduates, and 900 graduate students, and \$21 million in annual research funding. He has developed a strategic plan for the College of Engineering at UIC for the year 2010 which involves growing the college to 130 faculty, 1900 undergraduate students, 600 Ph.D and 400 M.S. students, and \$40 million in research funding. The key strategy that he has articulated is to have large interdisciplinary research projects in four areas: (1) Bio-technology (2) Materials and Nano-technology (3) Computing and Information

Technology (4) Energy, Environment and Infrastructure Technology. During the past two years, the UIC engineering faculty received four large center grants: \$5.5 million from MURI, \$3 million from NSF IGERT, \$2.5 million from NSF IGERT, and \$2 million from DARPA. In addition, the College has started a novel concept of Technology Centers which brings in shorter term research and development projects to industry. He has been successful in various fund raising initiatives for the College including a \$2 million Chair in Information Technology, three \$500,000 Professorships in Engineering, a \$500,000 Professorship in Energy Engineering, and a \$100,000 scholarship.

### **CONTRIBUTIONS AS AN ENTREPRENEUR**

Dr. Banerjee has founded a company called AccelChip, located in Schaumburg, Illinois ([www.accelchip.com](http://www.accelchip.com)) in July 2000. He served as its Founder, President and CEO until June 2002. During July, 2002 to June 2004, he transitioned to the role of Chief Scientist in a part time consulting role. The company has developed its first product called AccelFPGA which takes MATLAB and SIMULINK versions of DSP applications and map into field programmable gate arrays (FPGAs) This technology is based on the MATCH compiler technology developed at Northwestern University. Over the past two years he has hired a top management team, has raised \$2.3 million in Venture Capital funding, and produced over \$800,000 in revenues of its products, and grown the company to more than 20 employees. He was on leave from Northwestern University during 2001-2002, and has gone back to Northwestern as Chairman of the ECE department effective September 1, 2002. AccelChip was acquired by Xilinx Corporation in Jan. 2006 for \$21.5 million.

Dr. Banerjee has founded another company called BINACHIP, located in Glenview, Illinois ([www.binachip.com](http://www.binachip.com)) in July 2004. He is serving as Founder, Chairman and Chief Scientist of the company. BINACHIP is developing the BINACHIP-FPGA product that translates general purpose software binaries and assembly onto hardware implementations in the form of FPGAs. The technology is based on the FREEDOM compiler project developed at Northwestern University.